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Research Report

A Vertical Insulated Gate AlGaN/GaN Heterojunction Field-effect Transistor

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ABSTRACT We fabricated a vertical insulated gate AlGaN/GaN heterojunction field-effect transistor (HFET), using a free standing GaN substrate. This HFET has apertures through which the electron current vertically flows. These apertures were formed by dry etching the p-GaN layer below the gate electrodes and regrowing n^--GaN layer without mask. The HFET exhibited a specific on-resistance of as low as 2.6 mΩ·cm^2 with a threshold voltage of −16 V. This HFET would be a prototypes of a GaN-based high power switching device.

KEYWORDS AlGaN, GaN, Heterojunction, Heterostructure, Field-effect transistor (FET), Insulated gate, Vertical, GaN substrate

Gallium Nitride (GaN) has high critical electric field, high saturation velocity, and high thermal conductivity. In addition, AlGaN/GaN heterojunctions contain high two-dimensional electron gas (2DEG) with enhanced electron mobility. Owing to these attractive material properties, AlGaN/GaN heterojunction field-effect transistors (HFETs) have been intensively developed for high-power and high-frequency amplifies. These material properties indicate that the AlGaN/GaN HFET is also a promising candidate for post-Si high-power switching devices.

Vertical devices are more preferable than lateral ones for discrete high-power switching devices, because vertical ones are more area-efficient for both higher breakdown voltage and lower specific on-resistance. Moreover, there are some advantages of vertical ones over lateral ones. For example, it is easier to package vertical ones with heat release. Despite of these advantages, the previous works have been made on lateral ones. Several workers demonstrated the HFETs with vertical current aperture that were fabricated on a sapphire substrate.[1] Lately, free-standing GaN substrates have been commercially available, allowing us to develop vertical devices. There are only a very few reports on the vertical GaN-based devices.[2,3] However, the development of the vertical devices is quite primitive, making it impossible to evaluate the vertical device performance precisely.

In this work, we fabricated a vertical insulated gate AlGaN/GaN HFET, using a free-standing GaN substrate. We have first revealed the on-state characteristics of the vertical HFET. As a result, we obtained a specific on-resistance of as low as 2.6 mΩ·cm^2 with a threshold voltage of –16 V.

Figure 1 shows the schematic cross-sectional view of the vertical insulated gate AlGaN/GaN HFET. The electron current flows through the AlGaN/GaN heterojunction and the aperture. The Mg-doped p-GaN layer plays a role as a current blocking layer during the off-state. We employed an insulated gate, which allows higher voltage to be applied to the gate electrode and the gate leakage current to be reduced.

Figure 2 shows a process flow for forming the aperture. (a) A 3-μm-thick n^--GaN layer (Si : 1×10^{16} cm^{-3}), a 0.1-μm-thick p-GaN layer (Mg : 3×10^{19} cm^{-3}), a 10-nm-thick AlN layer, and a 50-nm-thick i-GaN layer were grown on a *c* - plane n^+-type GaN substrate by metal organic chemical vapor deposition (MOCVD). (b) The i-GaN/AlN/p-GaN was dry-etched by inductively coupled plasma (ICP) dry etching with Cl_2 gas using an SiO_2 mask. The etching depth was about 0.28 μm. (c) After the removal of the mask, a 0.3-μm-thick n^--GaN layer (Si: 1×10^{16} cm^{-3}) and a 15-nm-thick $Al_xGa1_{-x}N$ ($x \sim 0.25$) layer were grown.

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During this regrowth process, the AlN layer suppressed the upward diffusion of the Mg atoms in the p-GaN layer as well as the mass transport from the surface to the aperture region.(4) This regrowth process would lead to the planarized aperture.

The source regions were formed by Si ion implantation at an acceleration energy of 40 keV with a dose of 3×10^{15} cm^{-2} and the activation annealing at 1000ºC for 20 min with an SiO_2 encapsulated layer.

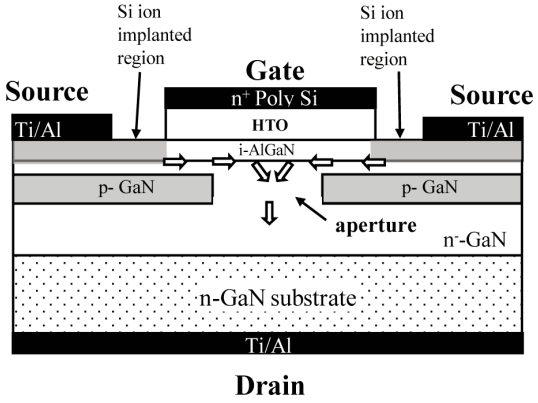

Fig. 1 Schematic cross-sectional view of the vertical insulated gate AlGaN/GaN HFET.

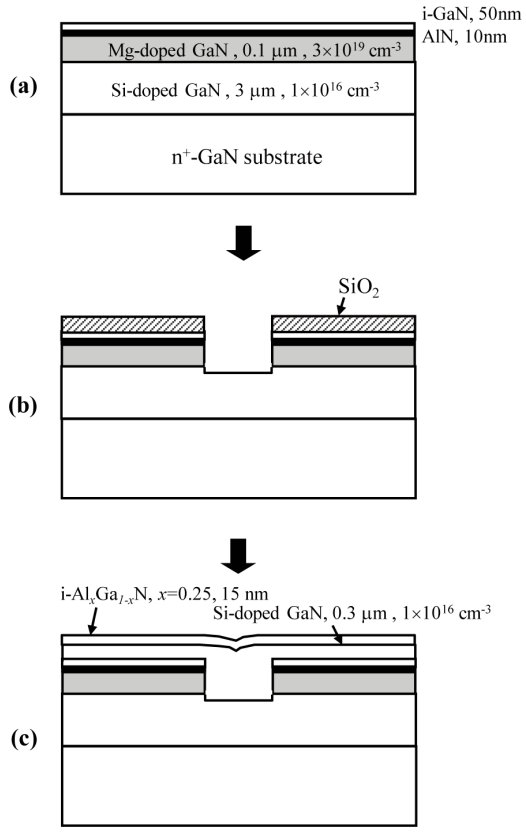

Fig. 2 Process flow for fabricating the aperture.

We obtained a specific contact resistance ρ_c of about $8 \times 10^{-5}\Omega \cdot cm^2$ with a circular transmission line method (c-TLM). The isolation region was formed by N_2^+ ion implantation at an acceleration energy of 30 keV with a dose of 5×10^{14} cm^{-2}. A 50-nm-thick high-temperature SiO_2 (HTO) layer as a gate insulator was deposited by low-pressure chemical vapor deposition (LPCVD). It was reported that the density of interface states of HTO/GaN was as low as 2×10^{11} eV^{-1}cm^{-2}.(5) A 250-nm-thick phosphorous-doped polycrystalline silicon (poly-Si) film as a gate electrode was deposited by LPCVD, followed by the activation annealing at 850ºC for 20 min in a nitrogen ambient. At the same time, the Mg in the p-GaN layer was activated. The poly-Si gate electrode was defined by dry-etching. A 500-nm-thick SiO_2 interlayer was deposited by plasma CVD and the contact holes were formed by dry-etching. Finally, the source and the drain electrodes Ti (20 nm)/Al (1 μm) were formed by electron beam (e-beam) evaporation.

Figure 3 shows a cross-sectional scanning electron microscope (SEM) micrograph of the fabricated HFET with an aperture width of 5 μm. In this micrograph, the white regions correspond to the p-GaN regions. This would be due to the charge-up induced during the SEM observation. Since there is a large band-bending of the cross-sectional plane of the p-GaN, the incident electrons would be accumulated in the cross-sectional plane. We found that the regrowing process of the 0.3-μm-thick GaN almost planarizes the 0.28-μm-deep trench region.

The measured HFET has two striped gate electrodes, a gate width of 40 μm × 2, a gate length of 2 μm, an aperture width of 3 μm, and an active area of 40 × 51 μm^2. **Figure 4** (a) shows the drain current (I_D) - the gate-to-source voltage (V_{GS}) characteristics at the drain-to-source voltage V_{DS} = 1 V. Here, I_D was defined

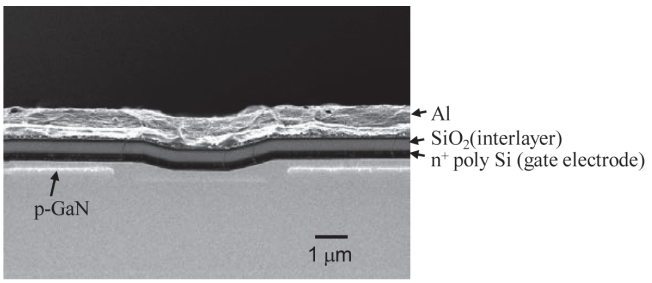

Fig. 3 Cross-sectional SEM micrograph of the fabricated HFET with an aperture width of 5 μm.

as the current density per active area. The HFET vertically operated with a threshold voltage of –16 V. Figure 4 (b) shows the subthreshold characteristics. The drain leakage current was of the order of 10^{-7} A/cm^2. This implies that the 0.1-μm-thick p-GaN layer played a role as the current blocking layer at V_{DS} = 1 V. On the other hand, we confirmed that the gate current (I_G) through the HTO was as low as 10^{-7} A/cm^2.

Figure 5 shows I_D-V_{DS} characteristics at V_{GS} = 0, –5, –10, and –15 V. No current offset was observed at V_{DS} ~ 0 V. This indicates that there were no barrier layers in the contact region as well as in the aperture region. We calculated the specific on-resistance R_{sp} from the linear region around V_{GS} = 0 V. As a result, R_{sp} was 2.6 mΩ·cm^2.

In order to apply the presented HFET to high-power switching devices, we have to improve the following four. (i) The p-GaN layer is needed to be thickened to play a role as the current blocking layer during the off-state (V_{DS} >> 1 V). (ii) It is necessary to make ohmic contacts on the p-GaN layer for high breakdown voltage. (iii) The n$^-$-GaN layer on the i-GaN was needed to be thinned, (0.3 μm → 0.1 μm). This leads to the depletion of the 2DEG with built-in potential of the p-GaN. We could achieve a normally-off, which is strongly preferable for power switching devices. (iv) The n$^-$-GaN layer as the drift layer is needed to be thickened. A 10-μm-thick n$^-$-GaN layer would be demanded for a 1-kV rated GaN power device. Attaining (i) - (ii), we could evaluate the breakdown voltage.

In conclusion, we fabricated an vertical insulated gate AlGaN/GaN HFET on a free-standing GaN substrate. The HFET exhibited the specific on-resistance of 2.6 mΩ·cm^2 with a threshold voltage of –16 V. We commented on the design considerations for the application of the HFET to high-power switching devices.

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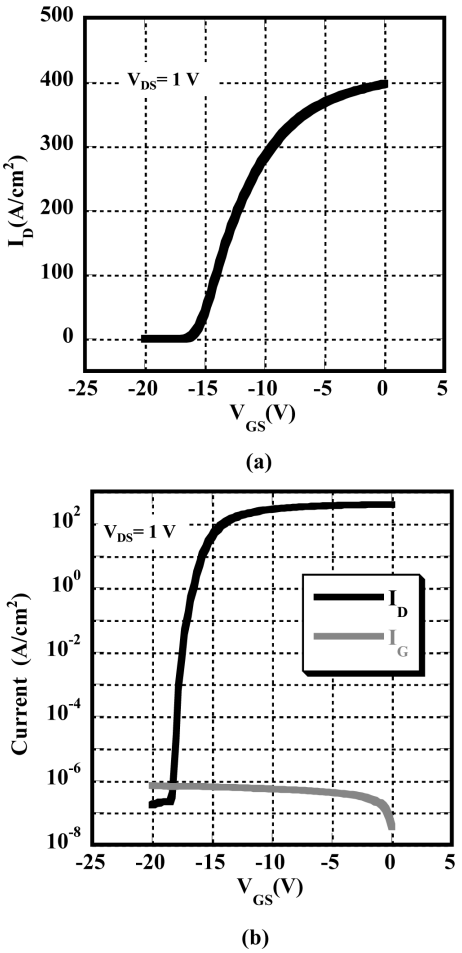

Fig. 4 I_D - V_{GS} characteristics at V_{DS} = 1 V. (a) Linear plot. (b) Single logarithmic plot.

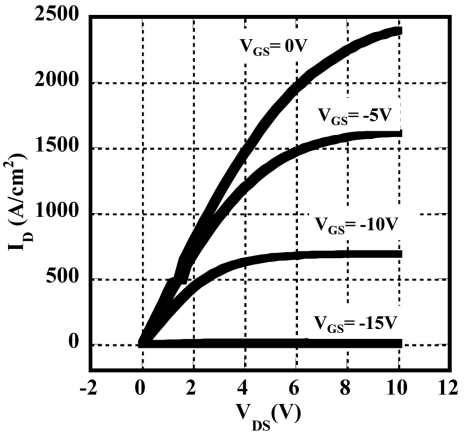

Fig. 5 I_D - V_{DS} characteristics at V_{GS} = 0, –5, –10, –15, and –20 V.

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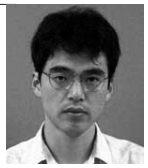

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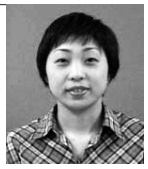

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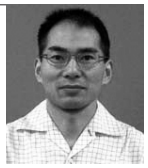

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