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Research Report

High-accuracy Temperature Prediction for an HV Inverter Using Electro-thermal Coupling Simulation

Takashi Kojima, Yuji Nishibe, Yasushi Yamada and Kaoru Torii

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ABSTRACT The present paper describes a novel RC compact thermal model capable of representing the thermal behavior of a multi-chip inverter module designed for use in hybrid vehicles (HVs). This RC compact thermal model can take into account lateral heat spreading within the modules and thermal interference among Si chips. The thermal model was validated through the comparison of temperature transient responses among the results calculated using the proposed model and FEM. Electro-thermal coupling simulation using this RC compact thermal model was carried out for the prediction of the IGBT chip temperature. This simulation method offers sufficient accuracy for prediction of the Si chip temperature in the HV inverter module under actual driving conditions. The worst-case error in the IGBT temperature is less than 5%.

KEYWORDS Circuit simulator, Inverter module, Compact thermal model, Hybrid vehicle, Electro-thermal coupling

1. Introduction

The high fuel efficiency and low emissions of hybrid vehicles (HVs) make these promising as environmentally friendly vehicles. The HV adjusts the driving force between the engine and an electric motor according to the running state of the vehicle. The main electrical components for the HV are a battery unit, an inverter unit, and an electric motor unit. The inverter is an important electrical component that converts the direct current from the battery into alternating current to rotate the motor. The Si devices (IGBT and diode) on the inverter module are the primary components of the inverter module and act as switching devices. Since Si devices generate a considerable amount of heat, a thermal problem, namely, the temperature increase of Si devices, must be taken into account in designing a highly reliable inverter module. In particular, the temperature increase of the Si devices during actual HV inverter operation is an important consideration. The power loss of the device, which is the source of the temperature increase, depends on the device temperature. The device temperature is determined by the cooling structure of the inverter module as well as the power loss of the device. Therefore, electro-thermal coupling simulation techniques, in which the calculation of the power loss and the temperature of the device should be coupled, become important for predicting the dynamic power loss and device temperature. The key point of this technique is the thermal model corresponding to the cooling structure. Conventional simulation techniques have no capability to estimate various performances of the HV inverter because of their insufficient thermal model.(1,2)

The present paper describes a novel compact thermal model that is suitable for electro-thermal coupling simulation of the HV inverter module and demonstrates the electro-thermal simulation technique, which can predict the dynamic temperature increase of Si devices by simulating the inverter operation in accordance with actual HV running.

2. Electro-thermal coupling simulation

In order to accurately evaluate the temperature increase of Si semiconductor chips, such as IGBT or diodes, which are embedded in the inverter module, the electro-thermal coupling simulation(3-6) is implemented in the circuit simulator of SIMPLORER.(7) The electro-thermal coupling simulation includes an electrical circuit model that represents the electrical behavior of the inverter, and an RC compact thermal model that represents the thermal behavior of the inverter module is prepared for the electro-thermal coupling simulation on the circuit simulator. **Figure 1** shows a diagram of the electro-thermal coupling simulation technique. The procedure for carrying out this technique is as follows. In the first step, the loss generated by a Si chip is calculated using the electrical circuit model. In the second step, the calculated loss is fed as the heat source into the RC compact thermal model, and the temperature increase of the Si chip is determined using the RC compact thermal model. In the third step, the determined temperature increase of the Si chip is fed into the electrical circuit model, and the corrected loss of the Si chip, which takes the temperature increase of the Si chip into consideration, is calculated. In the fourth step, the corrected loss is fed as the heat source into the RC compact thermal model, and the corrected temperature increase of the Si chip is determined again. The calculation flow described above is iterated.

The present paper focuses on the realization of the RC compact thermal model with a high accuracy, which is important in order to realize high-accuracy electro-thermal coupling simulation.

3. RC compact thermal model

The RC compact thermal model is a lumped parameter network represented by thermal resistance *R*, thermal capacitance *C*, and a current source equivalent to the heating source. The RC compact thermal model is needed in order to carry out electro-thermal coupling simulation because the RC compact thermal model can be easily implemented on a circuit simulator. A photograph of an example of a commercially available HV inverter module (multi-chip module) is shown in **Fig. 2**, in which several Si chips are packaged. **Figure 3** shows a cross section of the inverter module. The heat flux generated by heating each Si chip moves primarily from the Si chip to a convection cooler. In addition, the heat flux spreads in the lateral direction in the inverter module. The interference of each heating from each Si chip occurs among several Si chips, which contributes to the temperature increase of individual Si chips. Therefore, in order to construct an accurate RC compact thermal model, which models the thermal behavior of the inverter module, it is important to accurately understand the transient heat propagation behavior from the Si chip to the convection cooler and thermal interference behaviors among several Si chips due to the heat spreading in the module.

The circuit topology used as the RC compact thermal model is a Foster-type network, as shown in **Fig. 4**. The Foster-type network consists of parallel resistance and capacitance sub-circuits connected in series. Although the Foster network thermal model is a behavioral model that has no physical meaning with respect to *R* and *C*, this model has the advantages of

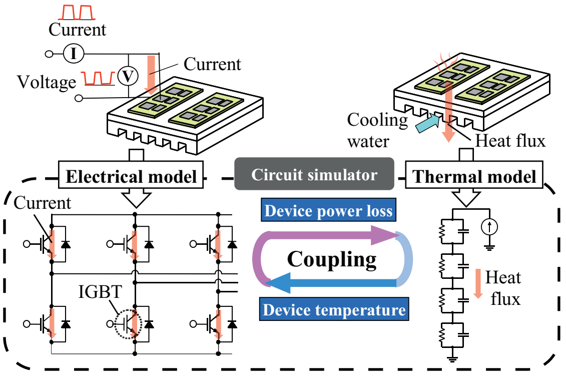

Fig. 1 Diagram of electro-thermal coupling simulation.

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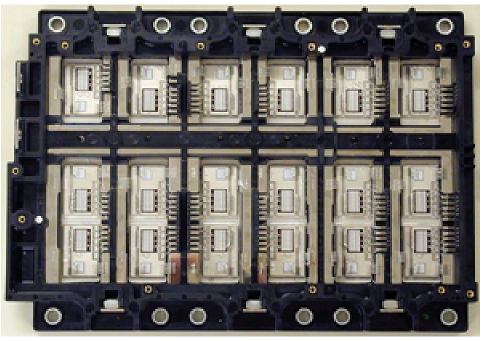

Fig. 2 Photograph of a commercially available HV inverter module.

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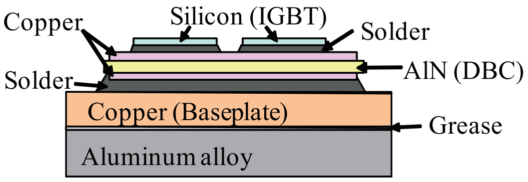

Fig. 3 Cross section of the inverter module.

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ease of RC parameter extraction and ease of expression of lateral thermal spreading, as compared to the conventional thermal model of the Cauer network circuit, as shown in **Fig. 5**, which has physical meanings for *R* and *C*. The one-dimensional Cauer network circuit cannot represent the lateral thermal spreading behavior of the inverter module, which has a three-dimensional structure.

Figure 6 shows temperature transient responses to the heat unit step for the Cauer and Foster network circuits. This figure indicates that the results calculated using the Foster network circuit are in agreement with the results calculated by the 3D-FEM.

The values of *R* and *C* in the RC compact thermal model are extracted in order to minimize the errors between the step temperature response profile calculated by FEM thermal analysis and that obtained by the RC compact thermal model using the least squares method. In the following section, the parameter extraction method is described in detail.

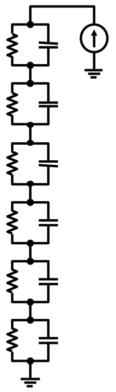

Fig. 4 Foster network.

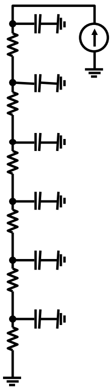

Fig. 5 Cauer network.

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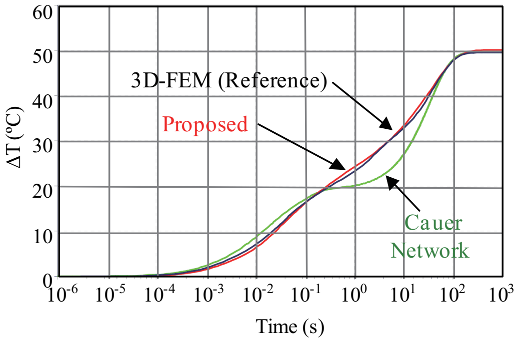

Fig. 6 Comparison of the calculated results for the proposed model, the Cauer network, and 3D-FEM for a step power response.

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The temperature distribution for the inverter module is shown in **Fig. 7**, for the case in which all of the Si chips have steady state heating. Figure 7 shows that all of the Si chips are found to exhibit thermal interference. The thermal impedance matrix is used to represent the thermal interferences among several Si chips inside the inverter module:

$$\begin{bmatrix} T_1 \\ T_2 \\ \vdots \\ T_j \\ \vdots \\ T_n \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \cdots & Z_{1j} & \cdots & Z_{1n} \\ Z_{21} & Z_{22} & \cdots & Z_{2j} & \cdots & Z_{2n} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ Z_{i1} & Z_{i2} & \cdots & Z_{ij} & \cdots & Z_{in} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ Z_{n1} & Z_{n2} & \cdots & Z_{nj} & \cdots & Z_{nn} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_i \\ \vdots \\ P_n \end{bmatrix} \quad \cdots\cdots (1)$$

where P_i is the loss generated by the i_{th} Si chip, and T_j is the temperature increase of the j_{th} Si chip. Here, T_j is related to P_i by the thermal impedance matrix element Z_{ij}, which indicates thermal interference between the i_{th} Si chip and the j_{th} Si chip. The diagonal element in the thermal impedance matrix, for example, Z_{ii}, represents the self heating of the i_{th} Si.

4. Determination of the RC thermal model parameters

The thermal impedance ($Z_{th}(t)$) of each physical domain can be expressed as follows:

$$Z_{th}(t)=R_1(1-\mathrm{e}^{-\frac{t}{R_1C_1}})+R_2(1-\mathrm{e}^{-\frac{t}{R_2C_2}}) \quad \cdots\cdots (2)$$

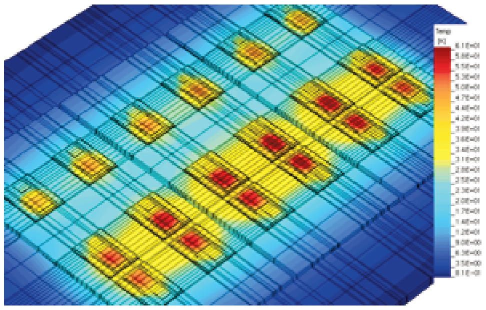

Fig. 7 Temperature distribution for the inverter module when all of the Si chips have steady state heating.

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The values of R_1, R_2, C_1, and C_2 are determined from the calculation results by 3D transient thermal FEM. In order to define these values, step heat generation is first applied to a Si chip, and the surface temperature increases of all of the Si chips and the temperature fixed points inside the module are observed. The temperature observation points are placed at the boundaries of physical domains, as shown in **Fig. 8**. The values of R and C are then determined by the least squares method to fit Eq. 2 to the FEM results. This procedure is repeatedly carried out for other Si chips considering the influence of the thermal interference. As a result, n^2 thermal impedances based on the Foster network are determined for n Si chips. These thermal impedances become the thermal impedance matrix elements. For example, Z_{ij} indicates the thermal impedances determined from the j_{th} Si chip temperature increase when step heat generation is applied to the i_{th} Si chip.

5. Results

The validity of the proposed RC thermal model is demonstrated for two examples of two different types of inverter module structures shown in **Figs**. 2 and **9**. An example of electro-thermal coupling is also demonstrated in order to validate the proposed RC compact thermal model under an actual HV running condition.

5. 1 Unit step responses

In this case, strong thermal interference occurs among four neighboring devices, as shown in Fig. 7. The temperature transient responses to the heat unit step calculated using the proposed compact thermal model is shown in **Fig. 10**. The results calculated using the proposed model are in agreement with the results calculated by the FEM for each device, indicating that the thermal interference is accurately modeled.

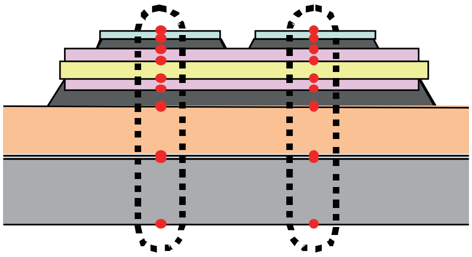

Fig. 8 Temperature observation points for determination of the RC thermal model parameters.

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5. 2 Periodic square-wave responses

Three IGBT chips and three diode chips are packaged on the same substrate in the inverter module, where the heating pattern with the periodical square wave is applied to the three IGBT chips and the inverted heating pattern to the three diode chips simultaneously, as shown in **Fig. 11**. In order to validate the applicability of the proposed model to thermal calculation of the inverter module, the frequency of the heating patterns is in the same range

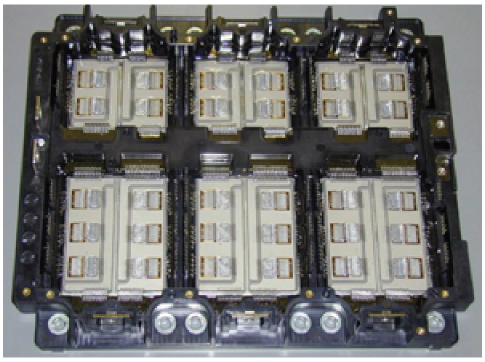

Fig. 9 Photograph of the test module used for validation of the proposed thermal model.

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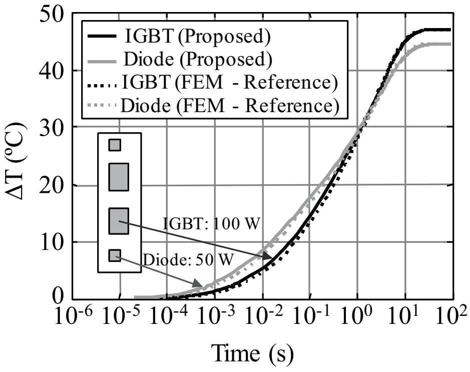

Fig. 10 Comparison of the calculated results for proposed model and 3D-FEM for a step power response with thermal interference.

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of working conditions as the motor frequency. **Figure 12** shows the temperature waveform for the IGBT chips as calculated by FEM thermal analysis and that obtained by the RC compact thermal model corresponding to this inverter module. Since the temperature waveform for IGBT chips calculated by the RC compact thermal model agrees with that calculated by FEM, the proposed RC compact thermal model is well suited to modeling the inverter module.

5. 3 Electro-thermal coupling simulation

A dynamic temperature prediction technique under actual driving condition was achieved in combination with the RC thermal compact model and the lookup table method. In the present study, we chose wide open throttle (WOT) operation as the real driving condition because this is a severe condition in terms of heat design.

5. 3. 1 Preparation of lookup tables

Circuit simulation using the power device model with transient behavior consumes a great deal of calculation time.(8) Therefore, we developed a method by which to prepare device power loss lookup tables. This lookup table method can reduce the calculation time. The parameters of the power loss lookup tables are the device current, the device temperature, and the DC-link voltage of the inverter. One of the best ways to obtain accurate lookup tables of power loss is to perform simulations using accurate simulation models (including the driving circuit of the power device, the smoothing capacitor on the power supply, and the stray inductance of the power module). The WOT operation simulation was able to be completed within a realistic calculation time using the developed lookup table method.

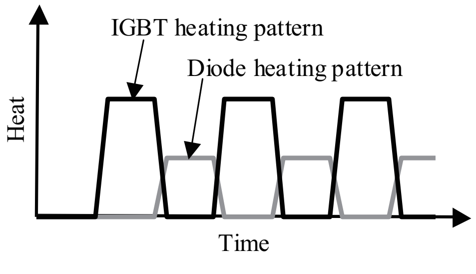

Fig. 11 Heating patterns of IGBT chips and diode chips.

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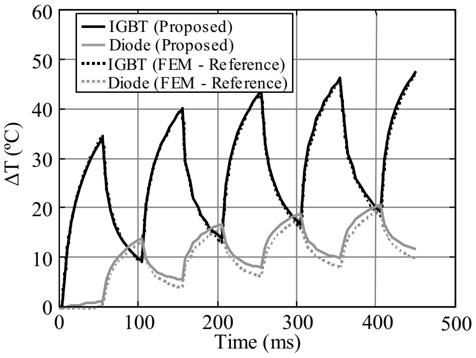
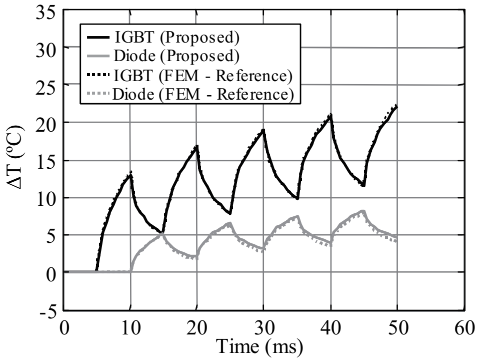
5. 3. 2 Technique for implementing the lookup table method in a circuit simulator

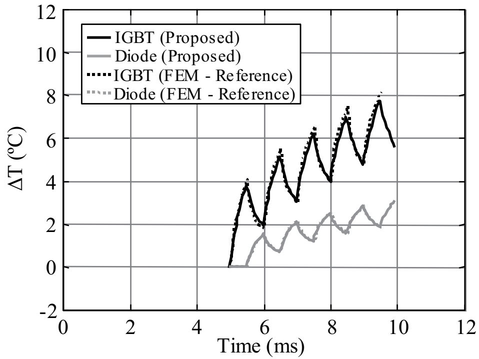
Electro-thermal coupling simulation was performed in order to predict the IGBT chip temperature in a 6-in-1 module, in which three IGBT chips and three diode chips are connected in parallel on each arm. In this simulation, the motor frequency is initially zero and increases monotonically. The simulation is



(a) Heating frequency: 10 Hz.



(b) Heating frequency: 100 Hz.



(c) Heating frequency: 1 kHz.

Fig. 12 Comparison of the calculated results for the proposed model and 3D-FEM for a periodic power response with thermal interference.

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finished when the motor torque begins to decrease. The following time-series data (see **Fig. 13**) are used as simulation conditions:

- Motor torque
- Motor frequency
- DC-link voltage of the inverter
- Carrier frequency of the inverter.

A block diagram of the electro-thermal coupling simulation is shown in **Fig. 14**. Power losses generated in power semiconductor devices are obtained from lookup tables. We implemented this block diagram in SIMPLORER.(7)

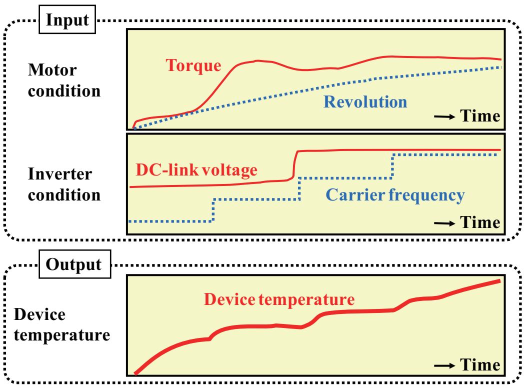

Fig. 13 Input and output of electro-thermal coupling simulation for an actual driving simulation.

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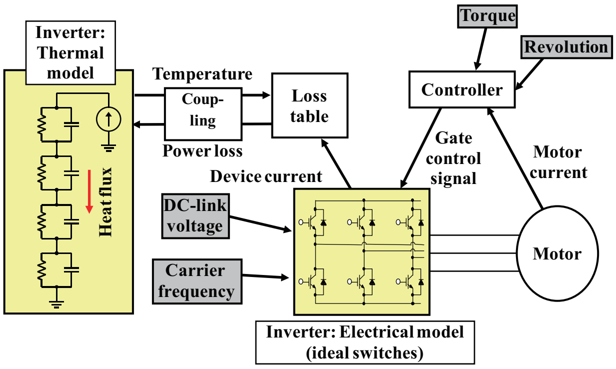

Fig. 14 Block diagram of electro-thermal coupling simulation.

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5. 3. 3 Accuracy verification of the lookup table method

The simulated and measured results are compared in order to determine the accuracy of the simulation technique in **Fig. 15**. Comparison of the simulated and measured results indicates that this method provides reasonable accuracy for the IGBT temperature estimation, as shown in the figure, in which the worst case error in the IGBT temperature is less than 5%. The fundamental advantage of this simulation technique is the shorter CPU time efficiency as compared to conventional electric-thermal coupling simulation. In the inverter simulation, the time step is chosen to be 1 μs, and it takes 210 minutes of calculation time to complete a 4-second WOT simulation.

Verification of the lookup table method for different driving patterns of the WOT operation was performed. **Figure 16** shows the simulation results for the temperature waveforms for several driving patterns. The most notable differences in the driving pattern are the slope angles of the tested road. The inverter temperature dependence of the HV system control pattern on the road condition can be calculated using different control signals, such as current, voltage, and career frequency. The simulation errors are less than 5%. The present study verified that models are practical tools for optimum inverter design in order to evaluate the inverter system performance under several driving conditions.

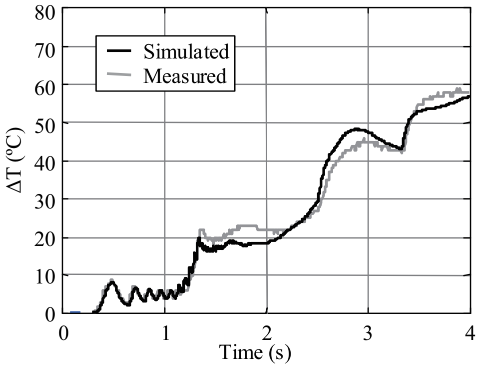

Fig. 15 Simulated temperature increase profile of the IGBT chip for WOT operation of an HV.

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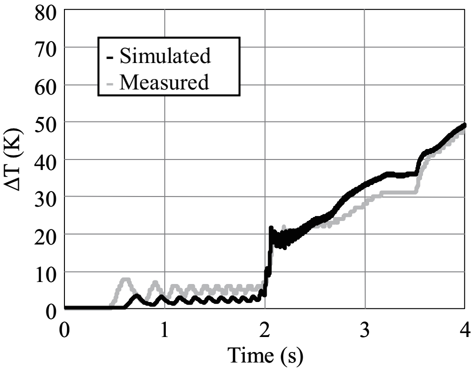
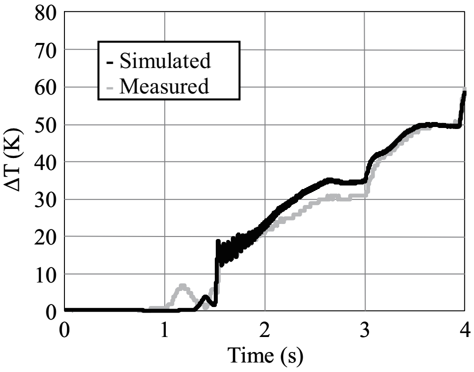
6. Conclusions

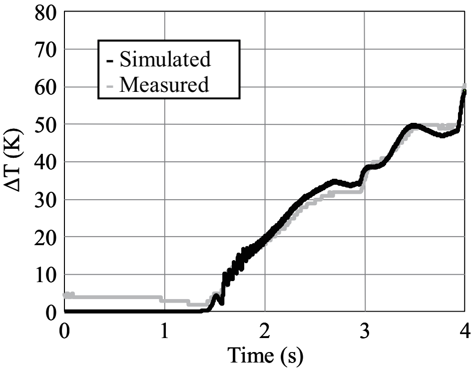
A novel RC compact thermal model that can accurately model the thermal behavior of a multi-chip inverter module for an HV was proposed. This RC compact thermal model uses the Foster network as the basic circuit configuration and the thermal impedance matrix to represent the thermal interference among the Si chips. Electro-thermal coupling simulation using this RC compact thermal model provides sufficient prediction accuracy regarding the Si chip temperature for the electrical and thermal design of the HV inverter module.



(a) Road condition A.



(b) Road condition B.



(c) Road condition C.

Fig. 16 Simulation results for IGBT temperature at WOT for several road conditions.

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Acknowledgments

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Takashi Kojima
Research Fields :
- Power electronics simulation
- Power device modeling
- EMC

Academic Degree : Dr. Eng.
Academic Society :
- The Institute of Electrical Engineers of Japan

Yuji Nishibe
Research Fields :
- Power device
- Electronic circuit
- Power module

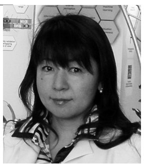
Academic Degree : Dr. Eng.
Academic Society :
- The Institute of Electrical Engineers of Japan

Award :
- MIDAD R&D Top 100 Selection Award, 2001

Yasushi Yamada*
Research Fields :
- Power module
- Power electronics simulation

Academic Degree : Dr. Eng.
Academic Societies :
- AIP
- The Institute of Electrical Engineers of Japan
- Society of Automotive Engineers of Japan
- ECS

Present Affiliation : Daido University



Kaoru Torii**
Research Fields :
- Power converter
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- Power electronics simulation
- EMC

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*Retired
**Toyota Motor Corporation