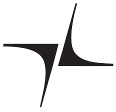

Special Review

Review

Current Status of Power Device Development

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ABSTRACT The current status of Si, SiC, and GaN power devices is reviewed. The performance of Si power MOSFETs and Si IGBTs continues to improve, even though these devices already have a long history. Recently developed device structures and the theoretical limit of on-resistance in Si power devices are discussed. High-performance SiC MOSFETs have been developed based on high-quality SiC substrates and epitaxial growth. These technologies and remaining issues for SiC MOSFETs are described. For GaN power devices, lateral structures have mainly been developed using Si substrates. Recently, however, vertical GaN devices using GaN substrates have been developed. Experimental performance is reviewed, and the remaining issues to be solved for both GaN device structures are discussed.

KEYWORDS Power Device, Si MOSFET, Si IGBT, SiC MOSFET, GaN HEMT, Lateral Device, Vertical Device

1. Introduction

Since the final decade of the 20th century, dwindling oil reserves and climate change have become serious global problems. For this reason, methods for reducing energy consumption and developing diverse renewable energy sources have become the focus of considerable attention. Electrical energy is the most common secondary energy used globally, so the reduction of electrical energy loss is highly desirable. Power electronics is a key technology for meeting this requirement because electrical energy flow can be controlled by the changing voltage and current to make them suitable for specific applications. As power devices are key elements in power electronics, and because their performance determines the total efficiency of power electronics systems, the development of high-performance power devices has attracted considerable attention. Si power devices have been in use for a long time, and their performance continues to improve. However, the performance of Si power devices is approaching the Si material limit. Therefore, wide-bandgap materials such as SiC and GaN have attracted notice, and SiC and GaN power devices have been developed. This paper discusses the current status of Si, SiC, and GaN power devices.

2. Theoretical Limits of On-resistance in Power Devices

Power devices have drift regions that sustain a high voltage in the off-state, as shown **Fig. 1**. In order to obtain a sufficient sustaining voltage, a thick drift layer is needed, which determines on-resistance R_{on} of the device. The R_{on} of the device can be described as follows:

$$R_{on} = R_{ch} + R_{JFET} + R_{D} + R_{sub}. \quad (1)$$

R_{ch} : Channel resistance
R_{JFET} : JFET resistance between p-type regions, as shown in Fig. 1
R_{D} : Drift region resistance
R_{sub} : Substrate resistance

To evaluate a material's potential for use in power devices, we generally assume $R_{ch} = R_{JFET} = R_{D} = 0$. In this case, the on-resistance of the devices is limited by the resistance of the drift region. The theoretical limit of the specific on-resistance of a device, therefore, can be calculated using Eq. (2), which does not include the channel resistance or other resistances.[1]

$$R_{on} = \frac{4V_B^2}{\mu_d \epsilon_s E_c^3} \quad (2)$$

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V_B : Breakdown voltage
μ_d : Electron mobility in the drift region
ϵ_S : Dielectric constant
E_c : Critical electric field for breakdown

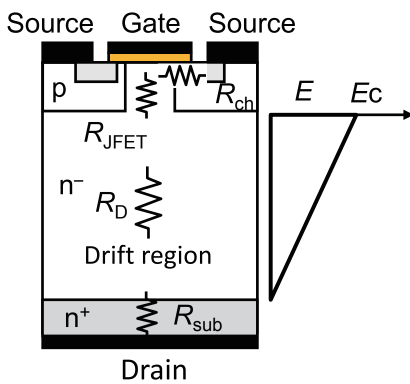
The physical parameters used are summarized in **Table 1**, and R_{on} values calculated using Eq. (2) are shown in **Fig. 2**. This figure shows the theoretical limits for Si, SiC, and GaN unipolar devices, and indicates that SiC and GaN have very high potential over a wide voltage range. An insulated gate bipolar transistor (IGBT) is also shown in Fig. 2, but the values shown were not calculated using Eq. (2) because the IGBT is a bipolar transistor that undergoes conductivity modulation, as will be described later.

3. Si Power Devices

Almost all of the power transistors used at the present time are made of Si, and many kinds of Si power devices have been developed, depending on the application. A range of Si power device applications is shown in **Fig. 3**, along with operating frequencies and power capacities. Recent mainly used power devices are power MOSFETs and IGBTs. Although these devices have long histories, their performance continues to improve. In this section, recent developments in power MOSFETs and IGBTs will be described.

3. 1 Power MOSFET

The power MOSFET is the most commonly used power device for medium- and low-power applications. Its superior properties are a high-speed response; that is, short turn-on and turn-off times, and high cost performance. On the other hand, power MOSFETs have a relatively high on-resistance compared with



$$R_{on} = R_{ch} + R_{JFET} + R_D + R_{sub}$$

Fig. 1 Electric field distribution in the drift region and resistances in power MOSFET.

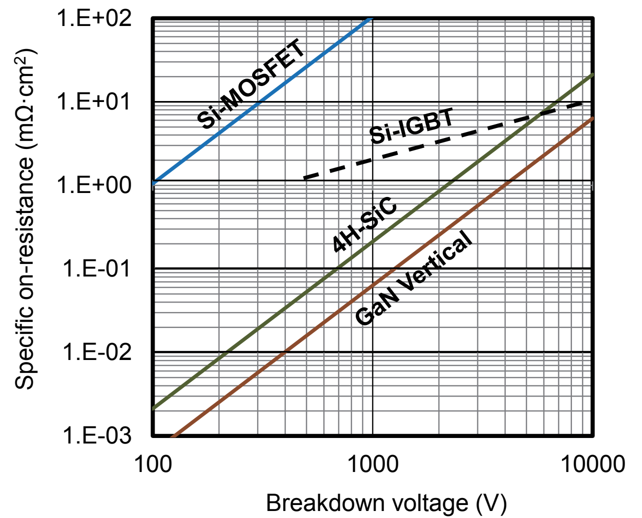


Fig. 2 Theoretical limit of R_{on} for Si, SiC, and GaN power devices.

Table 1 Material constants used in Eq. (1).

	ϵ_s	μ_d (cm²/Vs)	E_c (MV/cm)
Si	11.8	1350	0.3
4H-SiC	9.7	1000	2.8
GaN	9.0	1500	3.7

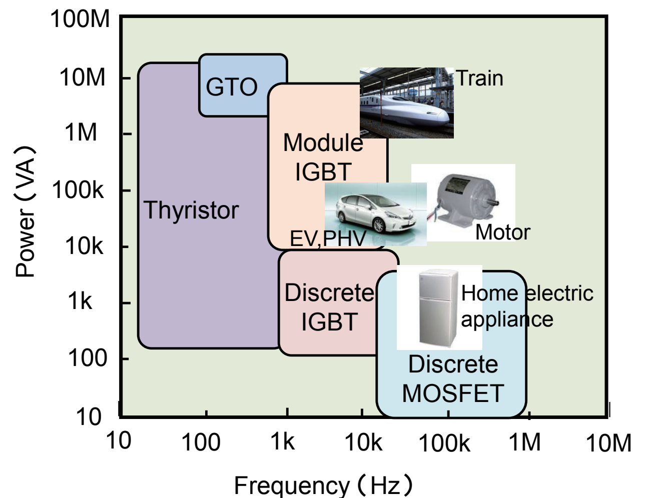


Fig. 3 Si power devices and their applications.

bipolar transistors, which limits their use in high-power applications. The device structure of a first-generation power MOSFET is shown in **Fig. 4**(a). This device is produced using a double diffusion process with p-type and n-type dopants, and is called a double-diffused MOSFET (DMOSFET). The channel is constructed on a p-type layer beneath the SiO_2 gate insulator. The creation of an inversion layer under the gate insulator is essential to normally-off operation of the device. This planar-type gate structure, however, restricts the ability to reduce the cell pitch and has R_{JFET} between p-type and n-type regions, resulting in a relatively high on-resistance. To overcome these weaknesses, the trench gate structure shown in Fig. 4(b) was developed. A trench through the p-type layer is formed by dry etching, and the side walls of the trench are used as gate channels. This structure therefore enables narrow cell pitches and no R_{JFET} is possible, which reduces the on-resistance. To further reduce the on-resistance, the remaining drift resistance must be reduced. In the conventional device structure, the source voltage in the off-state is maintained by depletion layer expansion from the p-type layer to the n-type drift layer. The electric field is highest at the pn junction under reverse bias conditions, which determines the drift layer thickness required to suppress the electric field E to below E_c for Si, and also determines the R_{on} as shown in Fig. 2. To overcome this limit, the electric field distribution in the drift layer must be changed from the triangular distribution shown in Fig. 1 to a square distribution. If a square distribution is achieved, a thinner drift layer can be used, and this will lead to a lower drift-layer resistance. Therefore, two types of drift structure have been developed: a super junction structure[2,3] and a field plate structure,[4-6] as shown in **Fig. 5**. In these structures, the depletion layer expands in the horizontal direction, and a flat distribution of E can be obtained. The Si MOSFET limit shown in Fig. 2 has been overcome by these drift structures. Furthermore, these structures have a low capacitance C_{gd} between the gate and the drain, which makes high-speed switching possible. The strongest advantage of power MOSFETs is their high cost performance, and they will probably remain the most commonly used power devices in the near future.

3. 2 Insulated Gate Bipolar Transistor (IGBT)

MOSFETs have been widely used for medium- and low-voltage applications, as discussed in the previous section. IGBTs were invented as a new power transistor with a low on-resistance, suitable for use in high-voltage switching applications. The basic device structure of an IGBT is shown in **Fig. 6.** The IGBT consists of a MOS channel part and a p-n-p bipolar transistor part. When the MOS channel turns on under a forward bias between the collector and emitter, holes are injected from the p-type collector in the device, which leads to a low on-resistance. This phenomenon is called conductivity modulation, and is unique to bipolar transistors. However, when the MOS channel turns off, the turn-off characteristics include a tail current that is caused by hole accumulation in the drift layer. The tail current results in a turn-off energy loss (E_{off}). The on-resistance of an IGBT is reduced

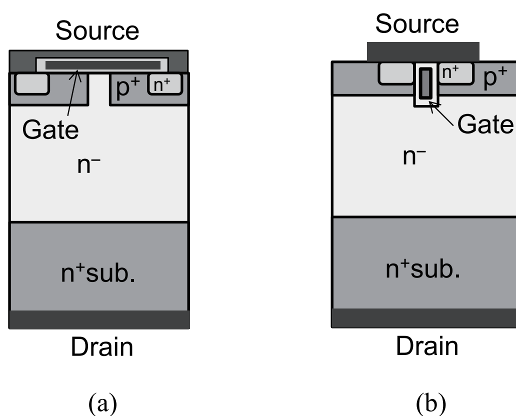


Fig. 4 Cross sectional structures of power MOSFETs, (a) double-diffused MOSFET and (b) trench gate MOSFET.

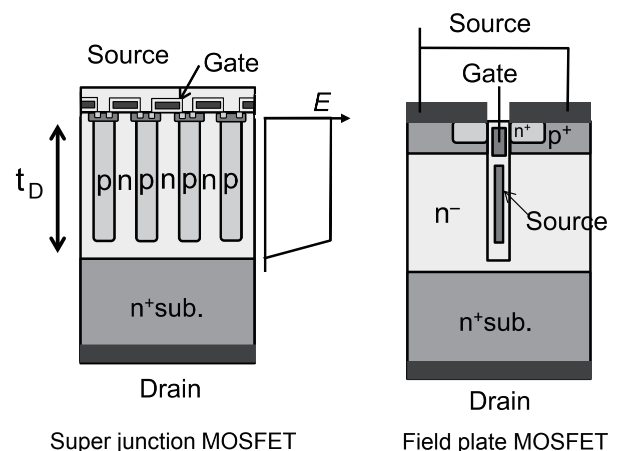


Fig. 5 Novel MOSFET device structures to obtain a low on-resistance.

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by increasing conductivity modulation. Consequently, there is a trade-off between R_{on} and E_{off}, and IGBT development involves improvement of this trade-off relationship. The gate structure has been changed from a planar gate to a trench gate, effectively lowering R_{on} by reducing the cell pitch, as has been done with power MOSFETs. The collector structure was also improved, as shown in **Fig. 7**, from that for the first generation of IGBTs.

A punch-through IGBT (PT-IGBT), as shown in Fig. 7(a), is produced on a p^+ substrate by epitaxial growth. In this structure, an n^+ layer is inserted on the p-type substrate and the electric field is stopped at the n^+ layer, which is called a field-stop layer. This structure permits a thinner drift layer than that for the first-generation IGBT shown in Fig. 6, resulting in a low R_{on}. On the other hand, a large number of holes are injected from the p^+ substrate to the drift layer in this structure, and the tail current increases. To reduce the tail current, defects have been introduced in the drift layer by proton implantation or electron beam irradiation. Unfortunately, this defect formation increases R_{on}.

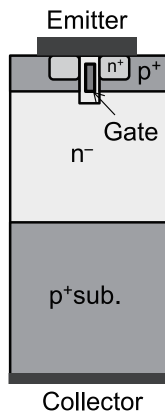

Fig. 6 Cross sectional structure of a first-generation IGBT.

To control hole injection, the non-punch-through IGBT (NPT-IGBT) shown in Fig. 7(b) was developed. This device uses a thin floating zone (FZ) wafer and a p^- collector layer formed by ion implantation to enable precise control of hole injection. The NPT-IGBT can reduce the tail current and results in a low E_{off}. However, as the NPT structure does not have a field-stop layer in the drift region, the drift layer must be sufficiently thick to prevent punch-through effects. The NPT-IGBT, therefore, has still weak point in R_{on}.

The newest type of IGBT, the field-stop IGBT (FS-IGBT), is shown in Fig. 7(c), and contains an n^+ field stop layer and a p^- collector formed by ion implantation into a thin wafer. This structure has a thin drift layer and enables precise hole injection control. The FS-IGBT has enabled drastic improvement of the trade-off relationship between R_{on} and E_{off}.

The theoretical limit of R_{on} for a MOSFET is determined by the drift-layer thickness. On the other hand, R_{on} for an IGBT is not limited by the drift-layer thickness because of the conductivity modulation. A high conductivity modulation leads to a low on-resistance. It would seem that R_{on} of the IGBT has no limit, but there is, of course, some limit, as has been discussed by Nakagawa.[7] In his paper, the relationship between the forward current density J and the forward voltage V_F was derived by integrating the following equation.

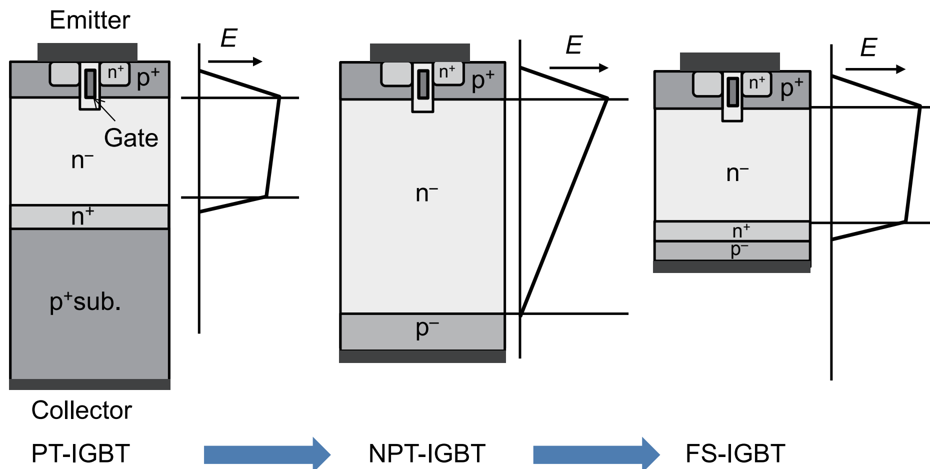

Fig. 7 Progress of IGBT structures to obtain low on-resistance and high switching speeds.

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$$J = 2qD_n \frac{\partial n}{\partial x} \tag{3}$$

n : Electron density in the drift region (cm^{-3})
D_n : Electron diffusion coefficient (cm^2/s)

The electron diffusion coefficient D_n can be approximated as

$$D_n = \frac{a}{n+b}\,. \tag{4}$$

a : Constant (3.7×10^{18} cm^{-3} for Si)
b : Constant (9.39×10^{16} s/cm for Si)

The final current-voltage relationship is given by

$$V_F = \frac{2kT}{q} \ln\left[\frac{1}{n_i}\left\{(n_0 + b)\exp\left(\frac{JW_i}{2qa}\right) - b\right\}\right] + R_{ch}J. \tag{5}$$

n_0 : Electron density at the collector-side drift region (cm^{-3})
n_i : Intrinsic carrier density for Si (cm^{-3})
W_i : Drift region width (cm)
R_{ch} : Channel resistance ($\Omega\cdot cm^2$)

The assumption adopted in Eq. (5) is that all of the current flows as electrons; that is, holes contribute only to the conductivity modulation.

We can obtain the theoretical R_{on} for each W_i using Eq. (5), which depends on the breakdown voltage as follows:

$$R_{on} = \frac{\partial V_F}{\partial J}. \tag{6}$$

The theoretical R_{on} for an IGBT based on Eq. (6) is shown in Fig. 2. This indicates that the IGBT also has a limited R_{on}, and Eq. (4) is responsible for IGBTs to have an R_{on} limit. This relationship indicates that the high carrier concentration induced by conductivity modulation reduces D_n, limiting the on-resistance. To approach the theoretical limit, suppression of the hole current is essential, and a narrow trench-to-trench structure was proposed in Ref. (6). Recently, an IGBT with a narrow trench spacing and a very low R_{on} of approximately 4 $m\Omega\cdot cm^2$ at 1.2 kV (close to the theoretical limit) has been reported.[8]

The performance of IGBTs continues to improve, and is approaching the theoretical limit. After considerable effort, modern IGBTs have a very high reliability and a high cost performance. Although new materials and devices could potentially exceed R_{on} of the IGBT limit, the cost barrier for the replacement of IGBTs will be high.

4. SiC MOSFET

The SiC-MOSFET was first fabricated on a 3C-SiC crystal on Si, and inversion operation of the MOSFET was achieved in 1987.[9] The performance was, however, insufficient because of the low quality of the SiC crystal. Recent high-performance SiC power devices have been achieved because of breakthroughs in the fabrication process. One such breakthrough, step-controlled epitaxy, was achieved by the Matsunami group[10] using a 6H-SiC substrate, and enabled the improvement of crystal quality. Step-controlled epitaxy produces superior single-crystal layers and allows for easy control of impurity doping. Step-controlled epitaxy utilizes off-angle substrates, and the growth mode on off-angle substrates can be explained using a stagnant layer model. The atoms diffuse to a surface, and can easily approach the steps formed during large off-angle processing, and two-dimensional nucleation and step-flow growth have been achieved, as shown in **Fig. 8**. Since the initial reports of step-controlled epitaxy, research on SiC MOSFETs has begun at many institutions. In the initial stage of SiC MOSFET development, 6H-SiC substrates were used. However, the substrate has since been changed to 4H-SiC because 4H-SiC has a higher electron mobility and a wider bandgap energy.

SiC substrate quality was also improved drastically by the rapid a-face (RAF) method.[11] This is the second important breakthrough in the SiC process. The RAF method uses alternative growth in the a- and c-directions, as shown in **Fig. 9**, which effectively eliminates threading dislocations from the grown bulk crystal. High-quality substrates produced using

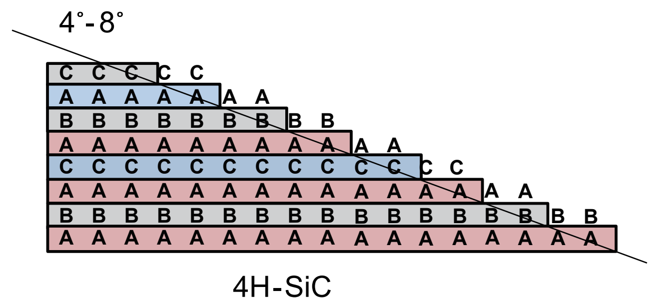

Fig. 8 Principle of step-controlled epitaxy of 4H-SiC.

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the RAF method will contribute not only to higher SiC device performance, but also to higher device reliability.

The recent progress of the SiC MOSFET has been very rapid, and high-performance devices have been reported from many institutes. MOSFETs with breakdown voltages of 1.2 kV and 3.3 kV at over 50 A have been developed,[12] and their application to the inverters of subway trains has been demonstrated. The device structure for SiC MOSFETs is typically very similar to that for Si MOSFETs, as shown in Fig. 4. However, the device fabrication process for the SiC MOSFET is very different from that of the Si MOSFET, because of the differences in material properties. The main process issues have been ion implantation, annealing, and oxidation. In the case of Si devices, implanted impurities can be made to diffuse to a predetermined depth by annealing. On the other hand, implanted impurities in SiC do not diffuse, even at high annealing temperatures. Moreover, a high accelerating voltage is needed for deep implantation. For example, a p-type base layer can be implanted to a depth of over 1 micron, which requires the accelerating voltage over 200 kV. Moreover, very high annealing temperatures of 1700-1800ºC are required for the activation of implanted impurities. Unfortunately, these high annealing temperatures induce surface roughness. However, this problem has been solved by the use of a carbon cap during annealing. Using this method, a very flat surface with a rms surface roughness of less than 1 nm rms has been obtained.[13]

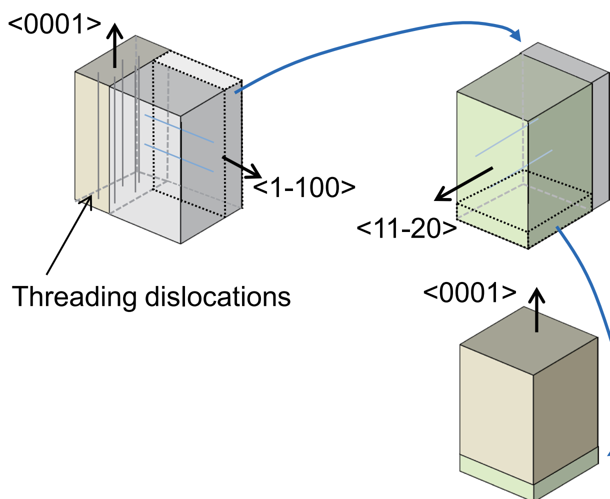

Fig. 9 Principle of the novel bulk crystal growth method called the rapid a-face (RAF) method.

Although a gate channel mobility of over 100 cm²/Vs is required to reduce the on-resistance, the channel mobility has been limited because of the high density of states at the SiO_2/SiC interface. The high interface state density issue has a long history, and various methods of oxide formation have been investigated. Initially, dry thermal oxidation was investigated. However, the channel mobility was low (1-11 cm²/Vs for 4H-SiC), and a high interface state density was observed. Pyrogenic gate oxidation was then investigated in 1996, and improvement of the channel mobility was reported for 6H-SiC.[14] This approach was also adopted for other faces: the (000-1) c-face and the (11-20) a-face with post-oxide H_2 annealing and high channel mobilities of 111 cm²/Vs[15] and 250 cm²/Vs[16] were obtained, respectively. This effect was caused by a reduction in the density of interface states near the conduction band edge.[17] However, for the (0001) Si face of 4H-SiC, this reduction effect was not observed. The next formation method investigated was the nitridation of the SiO_2/SiC interface after SiO_2 film formation using NO or N_2O gas.[18,19] This effectively increased the channel mobility of not only the (0001) Si-face but also the (000-1) c-face and the (11-20) a-face.[20] Nitridation treatment has become a standard gate-oxide formation process, although the channel mobility is typically only 30-40 cm²/Vs after the device fabrication process. $POCl_3$ treatment after oxide formation was also reported to be an effective treatment for the reduction of interface states.[21,22] Although various oxide formation methods were proposed and evaluated, no method has yet completely resolved the interface-related issues.

The gate oxide film also has reliability issues, such as a limited lifetime[23] and a threshold voltage shift.[24] Although these issues remain, appropriate device design and screening tests have made high voltage (1 kV - 3 kV), low on-resistance SiC MOSFETs possible.

5. GaN Power Devices

Before the year 2000, it was widely recognized that SiC would replace Si as a high-performance power device material. However, groundbreaking research was presented in 2001, when a team from the University of California at Santa Barbara and Yale University reported the high performance of an AlGaN/GaN based high-voltage transistor.[25] The

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breakdown voltage and specific on-resistance were 1.2 kV and 2 mΩ·cm^2, respectively. This impressively high breakdown voltage led to a surge of interest in GaN as an alternative to SiC for next-generation power devices.

Over the past decade, the performance of GaN power devices has rapidly improved. There are two types of devices currently being developed, with either a lateral or a vertical structure. At present, mainstream GaN power devices have a lateral structure, and many vendors have announced plans for the commercialization of such devices.(26) A lateral GaN power device with a blocking voltage of 600 V has high-performance characteristics, such as a low on-resistance and high-speed switching compared with Si power MOSFETs. On the other hand, although the high potential of GaN for vertical devices has been discussed,(27) progress in vertical devices has been slower than that for lateral devices. However, vertical devices have recently attracted additional research attention. In this section, the current status of lateral and vertical GaN power devices is presented.

5. 1 Lateral Structure Devices

Most GaN power devices being developed have a lateral structure. In general, a device with a lateral structure is not suitable for high-power switching applications because the breakdown voltage is determined by the gate-drain distance L_{gd}. In order to achieve a high breakdown voltage, L_{gd} should be large, which results in a high on-resistance. However, the unique characteristics of GaN allow a low on-resistance to be achieved even at high voltage. **Figure 10** shows the basic structure of a lateral GaN device, in which a two-dimensional electron gas (2DEG) is formed at the AlGaN/GaN interface. The 2DEG's high density of more than 10^{13} cm^{-2} in the drift region results in a low on-resistance device that maintains a high breakdown voltage. A high breakdown voltage of 2.2 kV has been reported for a GaN heterojunction field effect transistor (HFET) on an Si substrate.(28) However, the main target for the breakdown voltage is around 600 V because the 600 V range has the large market.

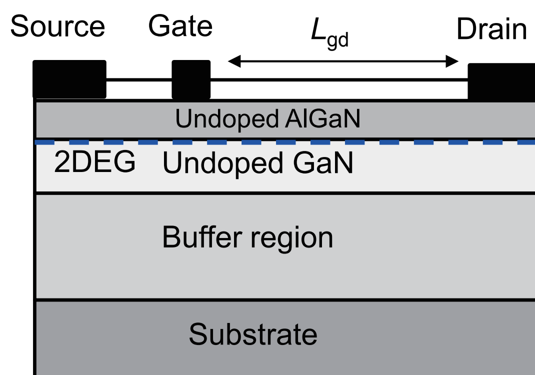

Fig. 10 Basic structure of a lateral GaN HEMT.

Another unique property is high-speed operation. The drift region consists of undoped AlGaN and GaN layers that provide a low feedback capacitance C_{gd}, making high-speed modulation possible. The low on-resistance and high-speed operation contribute to the high efficiency and compactness of power electronics modules.

One recent layer structure of such a device is GaN/AlGaN/AlN/GaN/buffer/substrate. The top GaN layer (2-5 nm thick) reduces the surface state density(29,30) and suppresses current collapse, as will be discussed later. A thin AlN (1-2 nm thick) layer is inserted at the AlGaN/GaN interface. This improves the electron mobility in the 2DEG because the AlN layer produces a high barrier, which reduces alloy scattering of electrons in the AlGaN layer. Si is the most commonly used substrate because it helps enable high cost performance. When an Si substrate is used, a buffer layer is essential for growing a high-quality GaN layer. The required thickness of the epitaxial layer is about 4 µm to guarantee a breakdown voltage of over 600 V. It is impossible to grow such a thick GaN layer without an adequate buffer layer, which relaxes the tensile stress in the epitaxial layer that arises from the difference between the thermal expansion coefficients of GaN and Si. Therefore, the buffer structure is the key to obtaining a high-quality epitaxial layer on Si. Individual epitaxial-wafer manufacturers have their own buffer structures based on AlN/GaN superlattices or pseudomorphic AlGaN layers. The present maximum diameter of the Si substrates used is 150 mm, and an epitaxial growth technology for 200 mm Si wafers is currently under development.

It is, however, widely recognized that there are two serious issues with lateral GaN devices: current collapse and normally-off operation.

Current collapse refers to a reduction in the drain current during high-voltage switching. Current collapse must be suppressed in order to apply GaN

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power devices to high-voltage switching. The phenomenon is caused by negative charges on the device surface[31] and/or in the AlGaN and GaN layers.[32,33] The negative charges reduce the 2DEG density in the drift region, resulting in increased on-resistance. The surface charges are redistributed from the gate to the device surface because of the high electric field concentration at the gate edge. Therefore, the use of a field plate can alleviate such electric field crowding.[34-37] An appropriate surface passivation film can also be employed to reduce the number of surface states that trap electrons.[38] A combination of these methods can effectively suppress current collapse. Another useful approach to reducing the surface state density is to form a thin GaN cap above the AlGaN layer, as mentioned above.[28] Another related issue is the large number of dislocations and point defects in the epitaxial layers, some of which can trap negative charges. An electron trap in bulk GaN has been evaluated from the on-resistance transient after a long trap-filling pulse.[39] The trap responsible for the current collapse had an activation energy of 1.03 eV, which is similar to that of a deep level that is possibly related to dislocations.[40] Therefore, improving the crystal quality is very effective in reducing the number of negative charges in the AlGaN/GaN structure.[41] The above measures allow current collapse to be suppressed for drain voltages of less than 600 V. However, a great deal of research is still being carried out in attempts to completely eliminate current collapse.

The second major issue with GaN power devices is achieving normally-off operation, since this is made difficult by the high-density 2DEG at the AlGaN/GaN interface. In Si and SiC power devices, a MOS channel usually uses an inversion layer, which results in normally-off operation. An inversion gate forms a threshold voltage of over 3 V, which is generally required to prevent noise-induced failure in the gate signal. Unfortunately, it is difficult to produce an inversion layer in GaN, and several alternative techniques for achieving normally-off operation have been proposed. These are summarized in **Fig. 11**.[42]

The proposed structure (a) shown in Fig. 11 involves a recessed-gate approach.[43] The AlGaN barrier layer (15-25 nm thick) below the gate is etched to a thickness of 2-5 nm, which causes the 2DEG to almost vanish in this region,[44] resulting in a positive shift of the threshold voltage. However, it is difficult to completely deplete the 2DEG to obtain a sufficiently high threshold voltage. If the recess is deep enough to penetrate the GaN layer, the 2DEG vanishes completely; this corresponds to a MOS gate structure. Normally-off operation was successfully achieved by this approach,[45] even without the use of a p-type GaN layer. The weak points of such a MOS structure are a high channel resistance and poor control of the threshold voltage.

The proposed structure (b) in Fig. 11 includes a p-GaN gate structure. This produces a depletion layer that extends from the p-n junction, thereby depleting the 2DEG, so that normally-off operation can be achieved.[46,47] However, in this structure, the gate bias voltage is higher than the built-in p-n potential, and this leads to a high gate leakage current. This makes it difficult to achieve a threshold voltage higher than the built-in potential. On the other hand, a group at Panasonic has developed a new type of transistor using a p-(Al)GaN gate, called the gate injection transistor

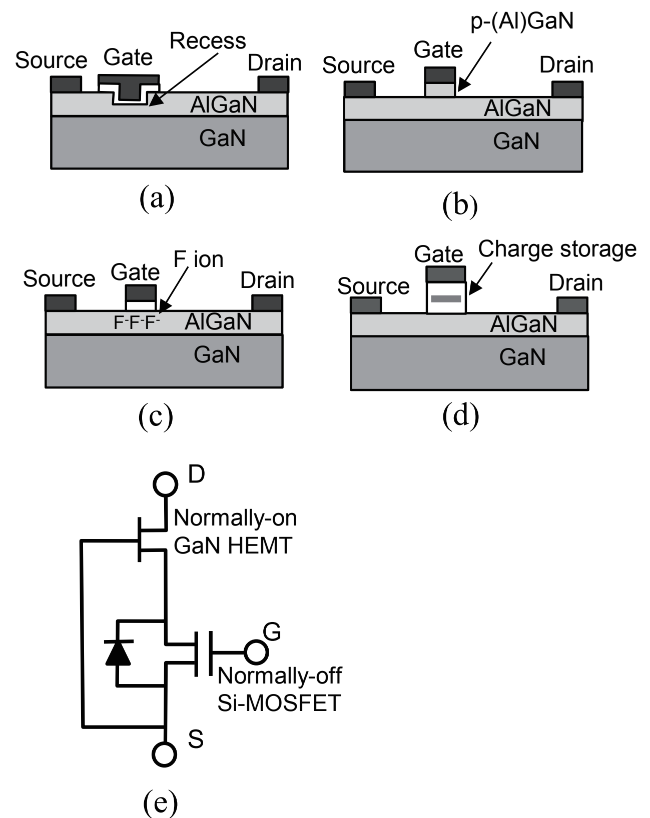

Fig. 11 Proposed normally-off device structures, (a) recessed gate structure, (b) p-(Al)GaN gate structure, (c) F ion implanted gate structure, (d) floating gate structure, and (e) cascode connection.

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(GIT).[46] They exploited hole injection from the p-(Al)GaN gate to the channel, which resulted in low on-resistance because of the conductivity modulation. In the fabrication of this device, the selective removal of the p-(Al)GaN layer is difficult. Dry etching control to stop the etching at the AlGaN barrier layer and the reduction of etching damage on the etched surface are issues that must be investigated.

The third approach (c) in Fig. 11 involves fluorine ion implantation into the AlGaN layer in the gate region. The negatively charged ions effectively deplete the 2DEG, thus achieving normally-off operation.[48] One technical difficulty is ensuring that no fluorine ions penetrate the GaN layer. If this occurs, the channel mobility deteriorates markedly.

The fourth structure (d) in Fig. 11 is a floating gate structure similar to that of flash memory.[49] The gate structure consists of a tunnel dielectric layer, a charge storage layer, and a blocking dielectric layer. Electrons are injected to the charge storage layer through the tunnel dielectric layer by the large positive bias of the control gate. The threshold voltage of the device is defined by the number of stored electrons. Although a high performance has been predicted for the floating gate structure,[50] its main problem is a short retention time.

Although normally-off operation has been realized with all of the above structures, the threshold voltages are around 1 V, which is lower than that of a conventional Si-MOSFET.

The final structure (e) for normally-off operation illustrated in Fig. 11 is a cascode connection using a high-voltage normally-on GaN HFET and a low-voltage normally-off Si-MOSFET.[51] In this configuration, the source of the Si-MOSFET is connected to the gate of the GaN HFET. Thereby, the gate-source voltage V_{GS} of the GaN HFET has a sign opposite to that of the drain-source voltage V_{DS} of the Si MOSFET. When the Si MOSFET switches off and the voltage across the device rises, this voltage switches off the GaN HFET. Conversely, when the Si-MOSFET switches on, the GaN HFET switches on as a response to V_{DS} of the Si-MOSFET dropping to a very low value. These two devices can be encapsulated in a single package to produce a three-terminal device. Since the threshold voltage is determined by the Si-MOSFET, this enables high threshold voltages (>3 V). This configuration is a realistic solution to obtaining a high threshold voltage. Although the on-resistance is the sum of the on-resistances of the two devices, a very efficient inverter based on cascade GaN HFETs has been achieved.[52]

5. 2 Vertical Structure Devices

The vertical structure has the advantages of a small chip size, easy wiring, a high breakdown voltage, and current-collapse-free operation. These characteristics are highly suited for high-power applications. We started the development of vertical GaN power devices in 2004. The first developed device structure is shown in **Fig. 12**, and is similar to the structure of a double-diffused Si MOSFET.[53] The electron current flows through the AlGaN/GaN heterojunction and an aperture at the center of the p-GaN layer. The p-GaN layer acts as a current blocking layer during the off-state. We employed an insulated gate, which allows higher voltages to be applied to the gate electrode and reduces the gate leakage current. The operation mode of this device was normally-on, with a threshold voltage –16 V, because the gate channel was an AlGaN/GaN heterostructure. The I_D-V_D characteristics are shown in **Fig. 13**. This was the first demonstration of a vertical GaN transistor.

Another device structure: a conventional trench MOSFET has also been examined, as shown in **Fig. 14**.[54] Trench MOSFETs are popular for Si and SiC power devices. However, for GaN, it was unknown whether or not a GaN trench sidewall could be used as a channel. At first, the trench was formed by ICP dry etching. The trench shape after dry etching was a V-shaped groove, and the sidewall of the trench was rough, as shown in **Fig. 15**(a). We

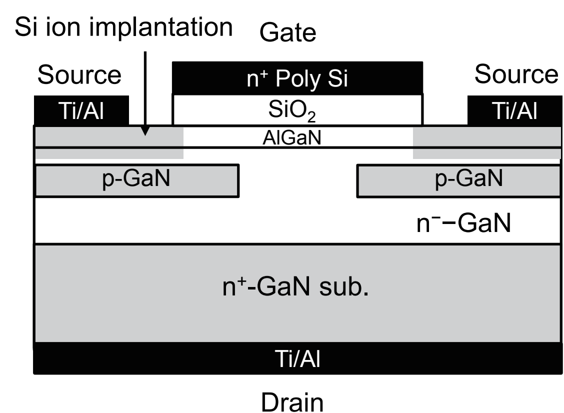

Fig. 12 Cross sectional structure of the first vertical GaN device.

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found that wet etching using tetramethylammonium hydride (TMAH) modified the dry-etched sidewall to be atomically flat, as shown in Fig. 15(b). A GaN trench MOSFET made by this novel trench fabrication technology was demonstrated. Other reports of vertical GaN devices fabricated on GaN substrates have also been published.(55-59) However, the device performance remains far below desired levels.

Through the fabrication of vertical GaN devices, we have revealed the development issues summarized in **Fig. 16**. The main issue is the quality of the GaN substrate. GaN substrates for blue laser applications made by hydride vapor phase epitaxy (HVPE) have been commercially available since the early 2000s. We evaluated GaN substrates by forming Schottky barrier diodes on them, and observed high leakage currents under low reverse voltages. Recently, new approaches to the fabrication of high quality GaN substrates have been developed. These are liquid-phase growth technologies: the ammonothermal method(60-62) and the Na flux method.(63-66) We evaluated a GaN substrate made by the Na flux method. The substrate was evaluated by measuring the leakage current and leakage points on pn diodes fabricated on the Na flux GaN substrate.(67) The evaluated diode structure and the leakage current are shown in **Fig. 17**. This diode had a breakdown voltage exceeding 1000 V. We examined the leakage points using an emission microscope. Four emission points, shown as arrows in **Fig. 18**(a), were observed under an 800 V reverse voltage. The emissions had broad spectra, indicating that they were due to hot electrons in the leakage currents. After the observation, the diode was etched to form etch pits originating from the dislocations in the epitaxial layer, using a mixture of acids ($H_2SO_4 : H_2PO_4 = 1 : 3$,

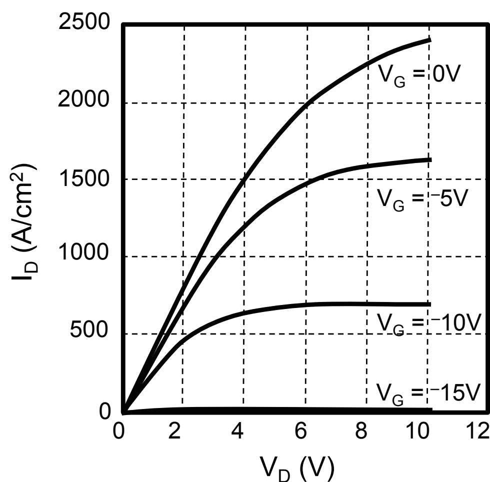

Fig. 13 I_D-V_D characteristics of the vertical GaN device shown in Fig. 12.

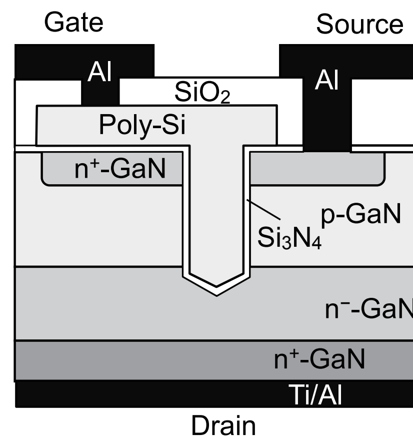

Fig. 14 Cross sectional structure of a trench gate vertical GaN device.

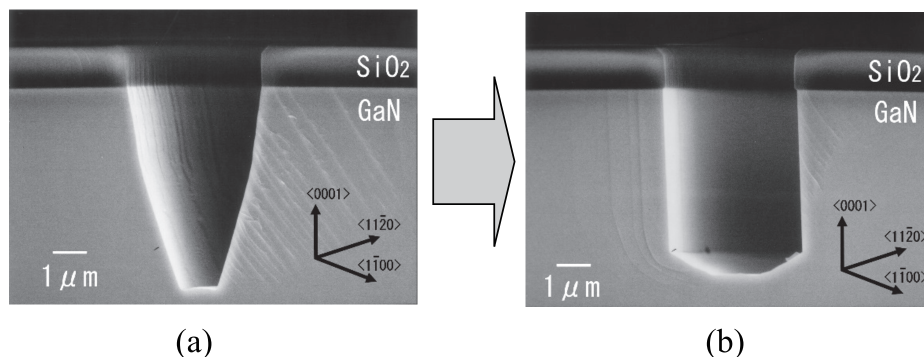

Fig. 15 Novel method for the fabrication of trench structure, (a) photo image of a trench after ICP dry etching, (b) photo image of a trench after additional wet etching of a dry etched trench.

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250°C). The etched surface is shown in Fig. 18(b). We compared Fig. 18(a) with Fig. 18(b) in detail and found that the leakage points did not coincide with etch pits. Moreover, the origins of the etch pits were examined by cross-sectional transmission electron microscopy (TEM). Edge and mixed (edge + screw) dislocations were observed beneath the etch pits. These results suggest that the edge and mixed dislocations are not the cause of the leakage current, which is consistent with previous reports on the electric characteristics of the dislocations.(68,69) Although no pure screw dislocations were found in this diode sample, screw dislocations would be conductive and would act as killer dislocations for high-voltage applications. However, the origin of the leakage current in Fig. 18 remains unclear. We predict, from measurements of other samples, that the origin is inclusions or dust particles near the pn junction that are included during epitaxial growth. Our evaluation indicates that the edge and mixed dislocations do not affect the leakage current under a high reverse voltage, and recent GaN substrates are of sufficient quality for research on high-voltage vertical devices. Recent research on diodes has also revealed that the quality of GaN substrates made by HVPE has become sufficient to enable their use in high-voltage devices.(70-72) However, the entire GaN substrate area does not yet have a uniform quality. Therefore, the remaining goals for GaN substrate development are larger samples of uniformly high quality, and dislocation reduction.

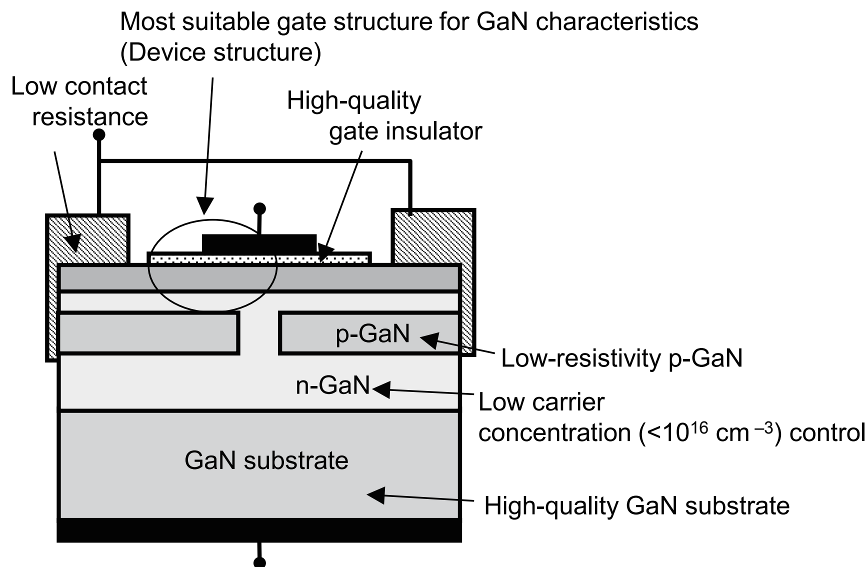

Fig. 16 Summary of issues for the development of a vertical GaN device fabrication process.

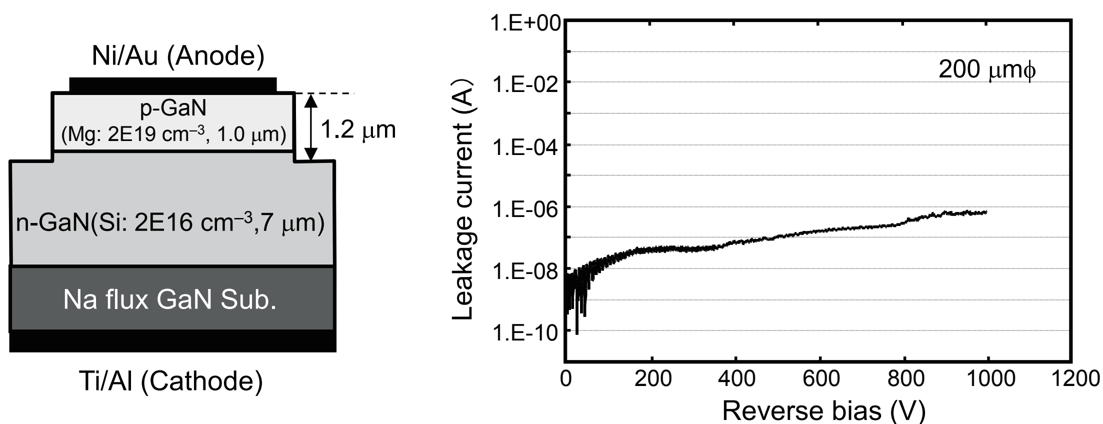

Fig. 17 Leakage current of a pn diode fabricated on a GaN substrate made with the Na flux method.

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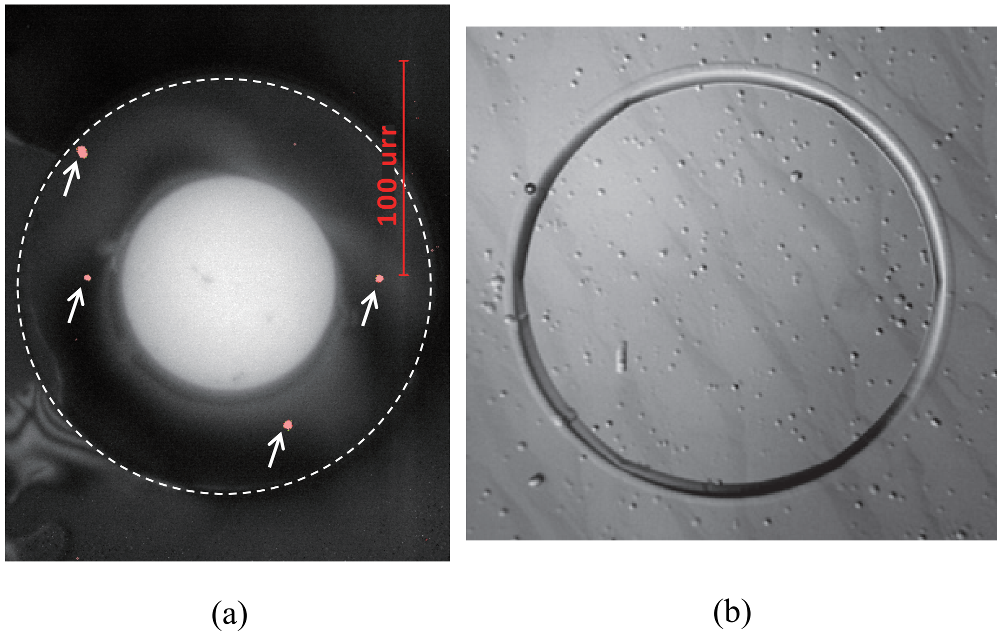

Fig. 18 (a) Photo image of a pn diode observed with an emission microscope. Emission points with arrows indicate the leakage points. (b) Photo image of a diode surface with etch pits caused by threading dislocations.

The next issue is low n-type doping control of the epitaxial layers. **Figure 19** shows the relationship between breakdown voltage and carrier concentration for various drift layer thicknesses. The figure shows that a carrier concentration of less than 1×10^{16} cm^{-3} is required for breakdown voltages over 3 kV. To obtain a low-carrier-concentration and low-resistive-drift layer, a high-quality crystal with few contaminants is necessary. However, epitaxial layers grown by MOCVD contain carbon atoms at concentrations of approximately 1×10^{16} cm^{-3}. These carbon atoms will compensate Si donors and result in a highly resistive epitaxial layer. The carbon atoms mainly come from the trimethylgallium (TMG) Ga source, and it is difficult to reduce the carbon contamination to below 1×10^{16} cm^{-3}. Therefore, epitaxial technology for growing highly pure GaN is essential for high-voltage devices. The next issue is related to p-GaN. It is difficult to fabricate a stable low-resistance p-type GaN layer. A low-resistance p-type layer is needed to ensure avalanche ruggedness of the device. It is difficult to control the characteristics of the p-type dopant Mg, such as a precise low concentration, up-diffusion, activation, and ohmic contact. A breakthrough in p-type GaN control is required. To address the issue of low contact resistance, as shown in Fig. 16, ion implantation is an effective method for producing a high-carrier-density thin layer under the ohmic electrode, which causes a low contact resistance. Ion implantation of the n-type dopants Si and Ge into GaN has been investigated,[73,74] and high levels

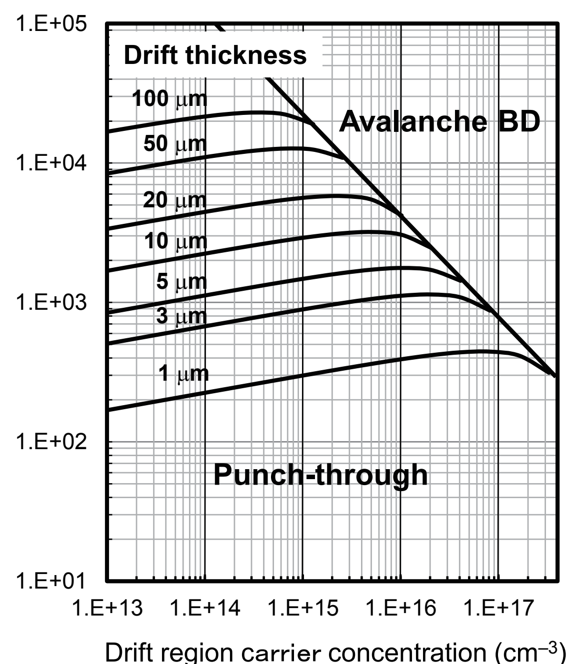

Fig. 19 Relationship between breakdown voltage and drift region carrier concentration for various drift thicknesses.

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of activation have been obtained. On the other hand, activation of the ion-implanted p-type dopants Mg and Be are difficult.[75,76] Achieving p-type ion implantation would simplify the fabrication process of vertical GaN devices. The final issue in Fig. 16 is the gate structure, which determines the device characteristics. The issues shown in Fig. 16 are still being investigated, but they have not yet been completely solved, since some of them are peculiar to vertical devices. To approach the theoretical performance limit, these issues must be overcome.

6. Summary

Si power devices are widely used in power electronics, and the technology continues to progress. Moreover, they have very high cost performance, and will continue to be used in the future. On the other hand, widegap semiconductor power devices have shown high performance, such as high breakdown voltages and low on-resistance. However, there are key issues to be solved for their practical application. If these issues are resolved and widegap semiconductor power devices demonstrate their performances, a new world of power electronics will open up.

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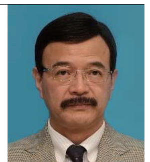

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