## Special Feature: Power Semiconductor Devices

*Research Report*

# Approaching the Limit of Switching Loss Reduction in Silicon Power Devices

Satoru Machida, Kenichi Ito and Yusuke Yamashita

*Report received on Jul. 29, 2015*

**ABSTRACT** This paper reports on the reduction limit of switching loss in silicon IGBTs. By measuring the gate resistance dependence of the turn-off surge and turn-off loss, a surge decrease and turn-off loss saturation at low gate resistance were observed. In addition, the surge decrease depended upon the temperature. To clarify the origin of the surge decrease, the internal dynamics during turn off were analyzed by device simulation. The simulation indicated that a dynamic avalanche occurs at the trench bottom during turn-off with at low gate resistance. This model based on the avalanche phenomenon can account for the measured dependence of the turn-off surge on gate resistance and temperature. This avalanche phenomenon can be suppressed by a reduction of the electric field and positive space charge near the trench bottom. A 20% improvement in the trade-off relationship between the turn-off loss and on-state voltage at low gate resistance, close to the turn-off loss limit, was realized by a structure with an additional P layer and an emitter trench. We conclude that suppression of the dynamic avalanche adjacent to the trench bottom plays a key role in turn-off loss reduction, especially at low gate resistances.

**KEYWORDS** Silicon Power Device, IGBT, Silicon Limit, Switching Loss, Dynamic Avalanche

## 1. Introduction

Silicon power devices are semiconductor devices for power electronics appliances. Insulated gate bipolar transistors (IGBTs) are widely used in medium-power applications such as household electric appliances and motor drives for hybrid vehicles because of their attractive features, which include low conduction loss, fast switching speed, and a wide safe operating area. Recently, a practical, theoretically-based approach at reaching the silicon IGBT performance limit has been attempted.[1-3] IGBTs with a narrow mesa trench have been fabricated based on the theoretical IGBT limit proposed in 2006.[4] The on-state voltage ($V_{ON}$) becomes lower with a narrower mesa due to internal excess carrier storage. A partially narrow mesa IGBT (PNM-IGBT), which has a narrow trench gate (less than 100 nm wide), was successfully fabricated by additional trench oxidation.[5] $V_{ON}$ almost reached the silicon limit. These approaches attempted to drastically reduce $V_{ON}$. However, IGBTs have a trade-off relationship between $V_{ON}$ and switching loss. Because of the increase in the internal excess carrier density with a narrower mesa, the storage time during turn-off is extended, resulting in an increased switching loss. Nevertheless, few papers have discussed the silicon IGBT limit from the viewpoint of switching loss.[6,7] In 2014, a shorted dummy-cell IGBT (SD-IGBT) achieved a 37% reduction in turn-off loss ($E_{OFF}$) to control carrier extraction.[8]

In order to approach the switching loss reduction limit, the possibility of achieving high-speed operation in silicon IGBTs should be investigated. This is because the switching loss becomes smaller at low gate resistance ($R_G$). Note that the turn-off surge voltage ($V_{SG}$) for silicon IGBTs decreases with decreasing $R_G$. This phenomenon may be peculiar to bipolar devices, as the $V_{SG}$ values of MOS devices continually increase as $R_G$ decreasing. In this $R_G$ region, the turn-off di/dt cannot be controlled by $R_G$, and this leads to saturates $E_{OFF}$. Therefore, the clarification of these phenomena in this region based on device physics is required to reach the switching loss limit.

This paper reports on the reduction limit of the switching loss in silicon IGBTs without increasing $V_{ON}$. In order to clarify the origin of the $V_{SG}$ decrease, the $R_G$ and temperature dependences of $V_{SG}$ were investigated. From the measured and simulated results, we found that the $V_{SG}$ decrease is derived from a dynamic avalanche adjacent to the trench bottom. This is called

 

a micro dynamic avalanche phenomenon. We assumed that this avalanche phenomenon was suppressed by the additional P layer at the bottom of the trench and the insertion of the emitter trench. As a result, the trade-off performance was improved by 20%, and the $E_{OFF}$ reduction limit was almost reached.

## 2. Experimental

To evaluate the $R_G$ and temperature dependences of $V_{SG}$, a 1.2 kV, 30 A Si power module was prepared. This module contained a field stop (FS) trench IGBT and PiN diode, serving as the switching device and free-wheeling diode (FWD), respectively. An inhomogeneous turn off due to gate signal delay should be considered in the case of a high internal gate resistance. However, this effect on $V_{SG}$ can be ignored because the internal gate resistance (less than 1 Ω) was sufficiently lower than the external gate resistances. Switching waveforms with different values of $R_G$ and temperature were measured with an inductive load in the double-pulse mode. The gate drive voltage, bus voltage, load inductance, and capacitance were 15/–7 V, 100 V, 100 μH, and 200 μF, respectively. The $R_G$ dependence of $V_{SG}$ was measured by adjusting the external resistance connected to the gate driver. The $V_{SG}$ dependence on temperature was obtained by adjusting the hot plate temperature and measuring the surface temperature of the devices with a thermocouple.

## 3. Analysis of Surge Voltage Decrease

**Figure 1** shows the measured $R_G$ dependence of $V_{SG}$ at various temperatures. The measured switching waveforms of the collector current ($I_C$) and collector to emitter voltage ($V_{CE}$) are shown the inset of Fig. 1. $V_{SG}$ is defined as the difference between the maximum voltage and the bus voltage. $V_{SG}$ increased as $R_G$ decreased from 150 to 60 Ω. However, $V_{SG}$ had a maximum value at approximately 60 Ω, and decreased at low $R_G$ as described in the previous section. In this study, we defined the regions of $V_{SG}$ decrease and increase with decreasing $R_G$ as Regions I and II, respectively, as depicted in Fig. 1. Note that $V_{SG}$ increased with increaseing temperature in Region I, whereas $V_{SG}$ was almost independent of temperature in Region II. The turn-off d$i$/d$t$ in Region I has already investigated, with a focus on the current components during the Miller plateau period.[9] It was concluded that the excess carrier sweep-out current, i.e., the "carrier streaming effect", plays an important role in Region I. However, the temperature dependence in Region I obtained in our study cannot be explained by the carrier streaming effect. This is because the amount of sweep-out current caused by the charging or discharging the depletion layer was almost independent of temperature.

The measured temperature and $R_G$ dependences of $V_{SG}$ were reproduced by device simulations. All simulations were carried out using the Sentaurus Device Simulator (Synopsys). The inset of **Fig. 2** shows the simulated $R_G$ dependence of $V_{SG}$ under the measurement conditions. $V_{SG}$ decreased at low $R_G$ values. To make the $V_{SG}$ decrease in Region I more pronounced, the bus voltage and collector current parameters were assigned different values from those in the measurement. Figure 2 shows a simulated $R_G$ dependence of $V_{SG}$ with changing temperature. In Region II, $V_{SG}$ was almost independent of temperature. On the other hand, in Region I, the surge voltage decreased with decreasing $R_G$ and increased with elevated temperature. The simulated results were in good agreement with the measurements.

To clarify the origin of the $V_{SG}$ decrease in Region I, the internal dynamics of the IGBT during turn off were investigated. **Figure 3** shows time evolutions of the carrier concentration, space charge, and avalanche

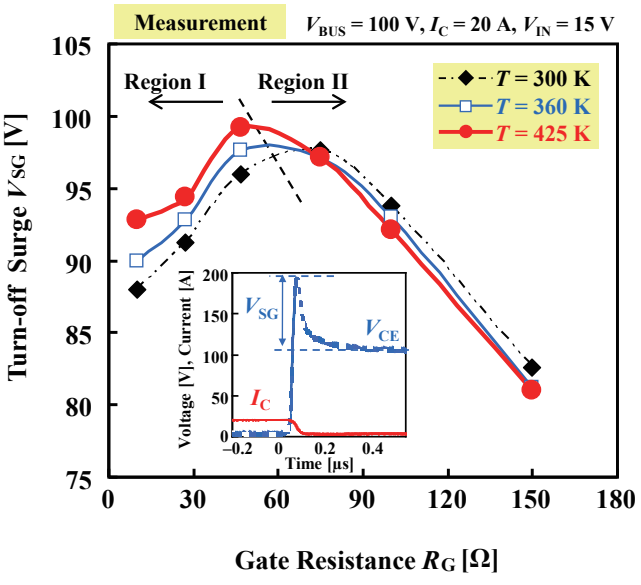


**Fig. 1** Measured dependence of turn-off surge on gate resistance and temperature. Inset: measured switching waveforms.

generation rate ($G_A$) at a location adjacent to the bottom of the trench when the maximum electric field in the device during turn off was observed. $G_A$ is given by the following equation:[10]

$$G_A = \frac{\alpha_n}{q}|J_n| + \frac{\alpha_p}{q}|J_p|, \quad (1)$$

where $\alpha_n$ and $\alpha_p$ are the ionization rates for electrons and holes, respectively, and $J_n$ and $J_p$ are the electron and hole current densities, respectively. In Region I, rapid increases in the positive space charge, carrier concentration, and $G_A$ occurred at the collector current turn-off ($t_{OFF}$).

These results indicate that a dynamic avalanche is generated near the trench bottom at time $t_{OFF}$. The origin of the $V_{SG}$ decrease is considered using a model we propose based on the dynamic avalanche phenomenon. **Figure 4** shows a schematic diagram of the internal space charges with different $R_G$ values at time $t_{OFF}$. The maximum electric field ($E_{max}$) near the bottom of the trench is mainly determined by the net space charge $Q = N_D + p - n$, where $N_D$, $p$, and $n$ are the donor, hole, and electron concentrations, respectively. In Region I, the electrons injected via the MOS channel into the depletion layer are negligible ($n \approx 0$) because the gate-to-emitter voltage is lower than $V_{th}$ after $t_{OFF}$ (see Fig. 3). In Region II, on the other hand, the MOS channel remains open and thus supplies electrons to the depletion layer ($n > 0$). Then, the net space charge in Region I becomes larger than in Region II ($Q_I > Q_{II}$), resulting in $E_{maxI} > E_{maxII}$. Because the ionization rate depends strongly on the electric field, $G_A$ in Region I becomes inherently higher than in Region II. This leads to a small turn off di/dt due to enhanced carrier generation. Thus, $V_{SG}$ decreases in Region I.

**Figure 5** shows the dependences of $V_{SG}$ and $G_A$ on $R_G$ and temperature at $t_{OFF}$. $G_A$ is very low in Region II, but increases with decreasing $R_G$ and temperature in Region I. This temperature dependence may be caused

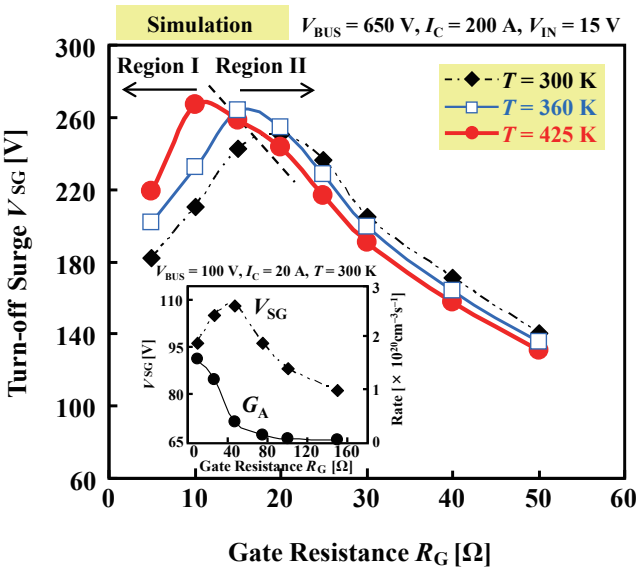


**Fig. 2** Simulated dependence of turn-off surge on gate resistance and temperature. Inset: simulated dependence of avalanche generation rate and turn-off surge on gate resistance under the same circuit parameters in the measurements.

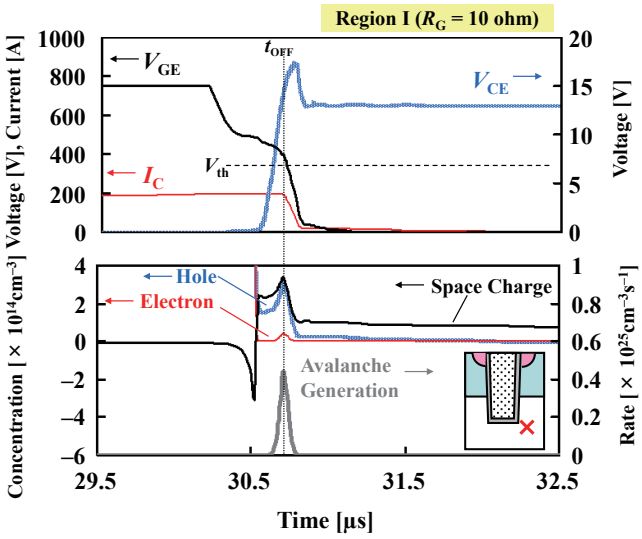


**Fig. 3** Simulated switching waveforms and internal dynamics adjacent to bottom of trench for Region I.

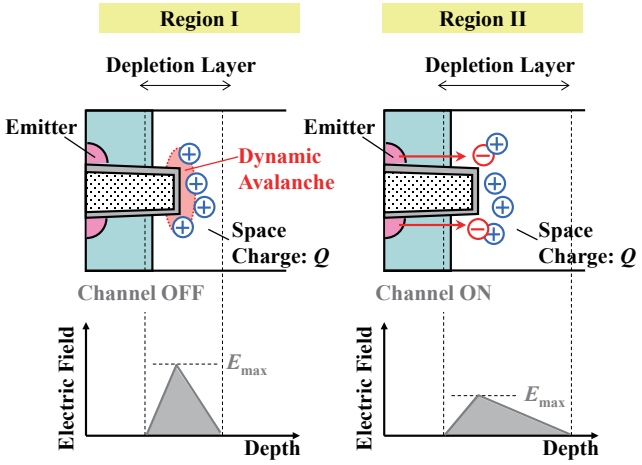


**Fig. 4** Schematic diagram of internal space charges at each region just before collector current turn-off.

by lattice vibrations. As expected, the decrease in $G_A$ with increasing temperature corresponds well with the temperature dependence of $V_{SG}$. Therefore, the $V_{SG}$ decrease is derived from the dynamic avalanche phenomenon and leads to $E_{OFF}$ saturation. This dynamic avalanche phenomenon occurs in a limited spatial region near the bottom of the trench. Moreover, the $V_{SG}$ decrease occurs even with an extremely small $G_A$ compared with that of the critical level, $G_{A\_crit} = 0.6 \times 10^{25}$ cm$^{-3}$s$^{-1}$, which was estimated by the collector current dependence of $E_{OFF}$.[6] Therefore, this phenomenon is called a "micro" dynamic avalanche.

## 4. Turn-off Loss Reduction Limit

From the above analysis, it was found that $E_{OFF}$ saturation is caused by a dynamic avalanche adjacent to the trench bottom. In this section, the limit to which $E_{OFF}$ can be reduced by the suppression of the dynamic avalanche will be considered. In order to estimate the $E_{OFF}$ reduction limit, a simple examination of the impact of avalanche generation on $V_{SG}$ decrease and $E_{OFF}$ saturation was performed by device simulation. **Figures 6** and **7** show the simulated $R_G$ dependence of $V_{SG}$ and $E_{OFF}$ with and without an avalanche generation model (default model: van Overstraeten), respectively.[11] Clearly, the $V_{SG}$ decrease disappears without the avalanche model. $V_{SG}$ continues to increase with decreasing $R_G$, similar to the behavior of MOS devices. Furthermore, the $E_{OFF}$ saturation at low $R_G$ also disappears without the avalanche model. Here, we take $E_{OFF}$ at $R_G = 0$ ohm without the avalanche model to be the $E_{OFF}$ reduction limit. Since the variations in the collector current ($di/dt$) and voltage ($dV/dt$) with time are extremely high, $E_{OFF}$ at its reduction limit mainly consists of power dissipation due to a current tail.

In order to approach the $E_{OFF}$ reduction limit, we attempted to enhance $V_{SG}$ intentionally by suppressing the dynamic avalanche. A reduction of the electric field and positive space charge near the trench bottom

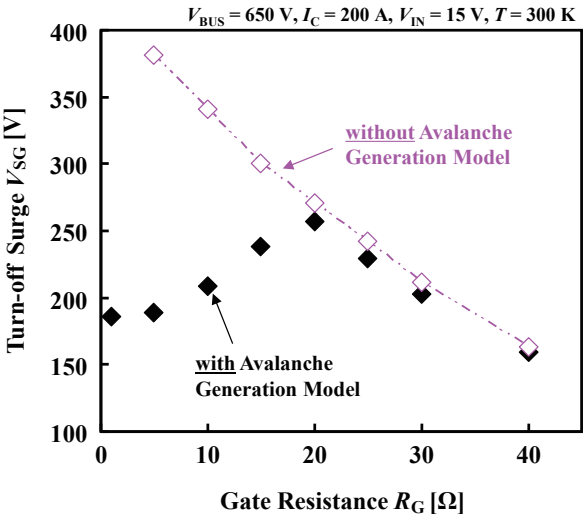


**Fig. 6** Simulated gate resistance dependence of turn-off surge with and without avalanche generation model.

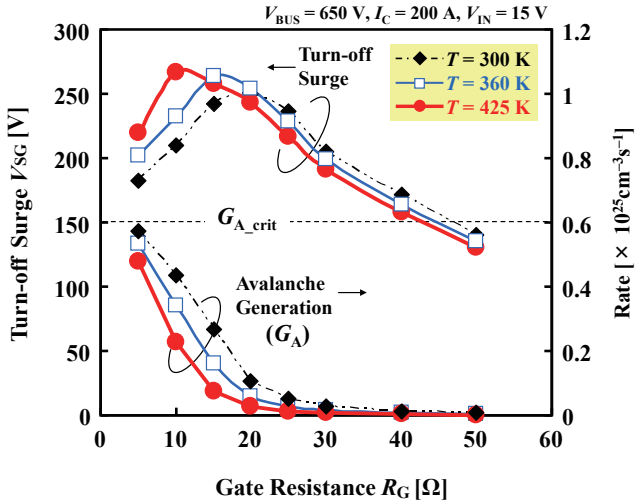


**Fig. 5** Simulated dependence of turn-off surge and avalanche generation rate on gate resistance and temperature.

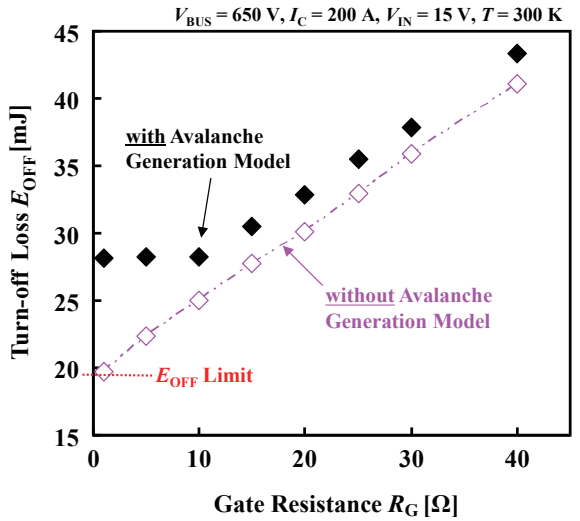


**Fig. 7** Simulated gate resistance dependence of turn-off loss with and without avalanche generation model.

should suppress the dynamic avalanche, as shown in Fig. 4. These physical quantities are strongly influenced by the device structure adjacent to the trench bottom. In order to confirm our proposed model and approach the $E_{OFF}$ reduction limit, the three device structures depicted in **Fig. 8** were simulated. The conventional FS-IGBT with a trench gate was used for reference (Device A). Device B has an additional P layer at the bottom of the trench gate. This P layer shields the electric field at the bottom of the trench during turn off. The electric field, which is reduced by the P layer, is partly applied to the pn junction between the p-body and n-base layer. Device C not only has a P layer at the bottom of the trench gate, but also has an additional trench connected to the emitter electrode (emitter trench). The insertion of an emitter trench has the following advantages over the other devices.

1) The emitter trench has little influence on $V_{ON}$.
2) The electric field near the bottom of the trench gate is reduced by the emitter trench.
3) Because the emitter trench is connected to ground, the electrostatic potential around the emitter trench becomes lower that ni a device without an emitter trench. Therefore, a partial dispersion of the hole current toward the emitter trench can also be expected.

These effects in Device C lead to the reduction of the electric field and positive space charge near the bottom of the trench gate. We predicted that the order of effectiveness at suppressing the dynamic avalanche would be Device C > Device B > Device A.

**Figure 9** shows the $R_G$ dependence of $V_{SG}$ for each device. Figure 9 also shows the $R_G$ dependence of $V_{SG}$ in Device A without the avalanche generation model. As expected, $V_{SG}$ decrease in Device B shrinks at low $R_G$. The improvement achieved for Device C is superior to that for Device B. **Figure 10** shows the $R_G$ dependence of $E_{OFF}$ for each device. $E_{OFF}$ reduction corresponds to a shrinkage of the $V_{SG}$ decrease at low $R_G$. **Figure 11** shows the trade-off curve with $R_G$ = 1 Ω for each device. The trade-off performance in Devices B and C is improved by 9% and 20%, respectively, without increasing $V_{ON}$. As a result, $E_{OFF}$ in Device C is close to the reduction limit (30%). In this study, it became clear that suppression of the dynamic avalanche near the trench bottom significantly contributes to $E_{OFF}$ reduction. However, $E_{OFF}$ still does not reach its lower limit, as shown in Fig. 11. This indicates that further suppression of the dynamic avalanche is required. Moreover, an extremely high $V_{SG}$ at low $R_G$, as shown in Fig. 9, may cause a narrowing of the safe operating area even with a low stray inductance. As future work, we will investigate improved device robustness and additional $E_{OFF}$ reduction.

## 5. Conclusion

In summary, the switching loss limit in silicon IGBTs was investigated. From the measured $R_G$ dependence

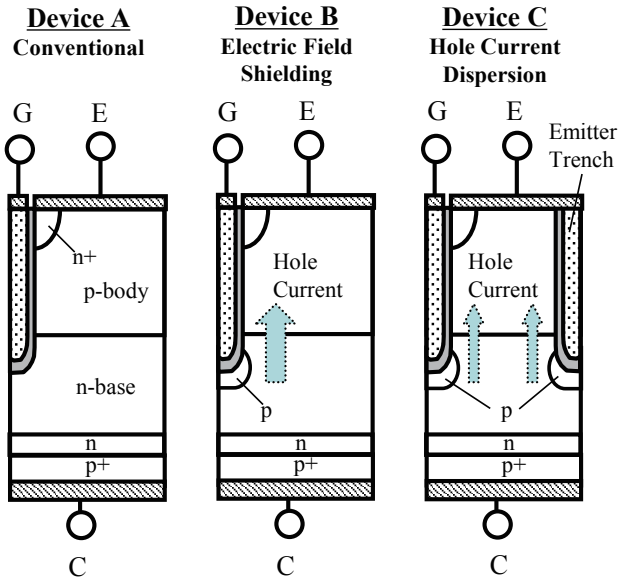


**Fig. 8** Simulated device structures for suppression of dynamic avalanche near gate trench bottom.

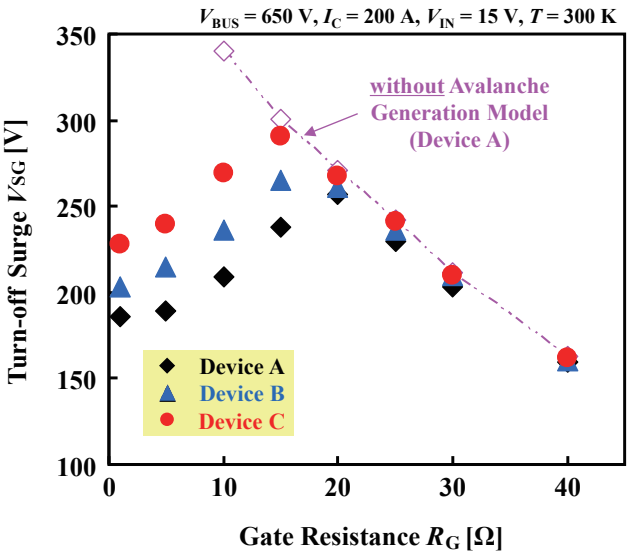


**Fig. 9** Simulated gate resistance dependence of turn-off surge with each device.

of $V_{SG}$ and $E_{OFF}$, $V_{SG}$ decrease and $E_{OFF}$ saturation at low $R_G$ was observed. Moreover, the $V_{SG}$ decrease depends on the temperature. To clarify the origin of the $V_{SG}$ decrease, the internal dynamics during turn off were analyzed by device simulation. The simulations indicated that a dynamic avalanche occurs at the trench bottom during turn-off at low $R_G$. This model based on the avalanche phenomenon can account for the measured dependences of $V_{SG}$ on $R_G$ and temperature. This avalanche phenomenon is suppressed by the reduction of the electric field and positive space charge near the trench bottom. A 20% improvement in the trade-off relationship between $E_{OFF}$ and $V_{ON}$ at low $R_G$ was realized and the $E_{OFF}$ limit was almost reached by a structure with an additional P layer and an emitter trench. We conclude that suppression of the dynamic avalanche adjacent to the trench bottom plays a key role in $E_{OFF}$ reduction, especially at low $R_G$.

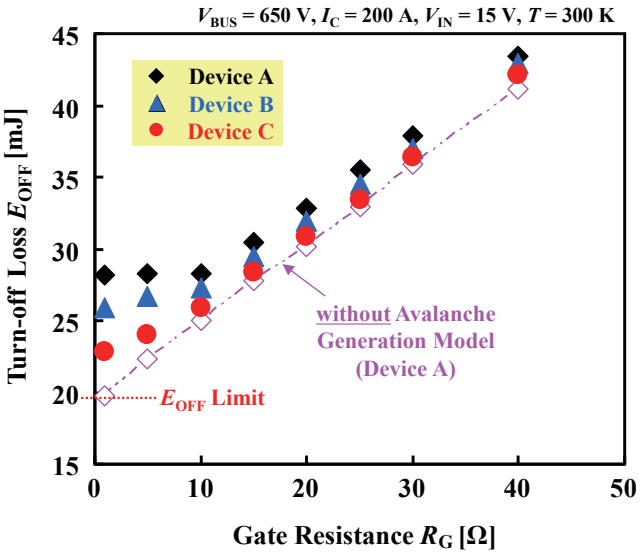


**Fig. 10** Simulated gate resistance dependence of turn-off loss with each device.

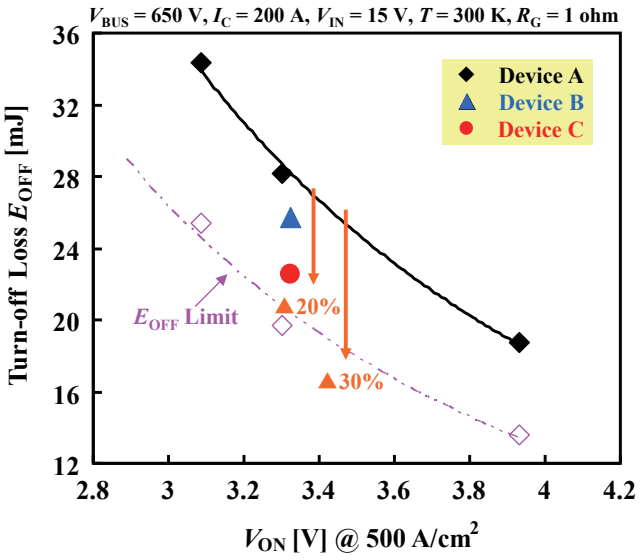


**Fig. 11** Simulated trade-off relation between on-state voltage and turn-off loss with each device.

## References

(1) Nakagawa, A., Kawaguchi, Y. and Nakamura, K., "Power Device Evolution Challenging to Silicon Material Limit", *Ext. Abstr. of Int. Conf. on Solid State Devices and Mater.* (2008), pp. 732-733, The Japan Society of Applied Physics.

(2) Nakagawa, A., "Recent Advancement in High Voltage Power Devices and ICs", *Proc. of IEEE 17th VLSI Technol., Systems and Appl.* (2008), pp. 103-104.

(3) Takei, M., Fujikake, S., Nakazawa, H., Naito, T., Kawashima, T., Shimoyama, K. and Kuribayashi, H., "DB (Dielectric Barrier) IGBT with Extreme Injection Enhancement", *Proc. of IEEE 22nd Int. Symp. on Power Semiconductor Devices and ICs* (2010), pp. 383-386.

(4) Nakagawa, A., "Theoretical Investigation of Silicon Limit Characteristics of IGBT", *Proc. of IEEE 18th Int. Symp. on Power Semicond. Devices and ICs* (2006), pp. 5-8.

(5) Sumitomo, M., Asai, J., Sakane, H., Arakawa, K., Higuchi, Y. and Matsui, M., "Low Loss IGBT with Partially Narrow Mesa Structure (PNM-IGBT)", *Proc. of IEEE 24th Int. Symp. on Power Semicond. Devices and ICs* (2012), pp. 17-20.

(6) Machida, S., Ito, K. and Yamashita, Y.,"Micro Dynamic Avalanche Phenomenon during Turn-off in Si-IGBTs", *Jpn. J. Appl. Phys.*, Vol. 53 (2014), 04EP01.

(7) Machida, S., Ito, K. and Yamashita, Y., "Approaching the Limit of Switching Loss Reduction in Si-IGBTs", *Proc. of IEEE 26th Int. Symp. on Power Semiconductor Devices and ICs* (2014), pp. 107-110.

(8) Gejo, R., Ogura, T., Misu, S., Nakamura, K., Yasuhara, N. and Takano, A., "Ideal Carrier Profile Control for High-speed Switching of 1200 V IGBTs", *Proc. of IEEE 26th Int. Symp. on Power Semicond. Devices and ICs* (2014), pp. 99-102,.

(9) Onozawa, Y., Otsuki, M., and Seki, Y., "Investigation of Carrier Streaming Effect for the Low Spike Fast IGBT Turn-off", *Proc. of IEEE 18th Int. Symp. on Power Semicond. Devices and ICs* (2006), pp. 173-176.

(10) Sze, S. M., *Phys. of Semicond. Devices* (2007), Chap. 4, Wiley, New York.

(11) *Sentaurus Device User Guide* (Version F-2011.09, 2011), Chap. 16, Synopsys. Inc.

 

**Satoru Machida**
Research Field:
- Power Semiconductor Devices

Academic Degree: Dr.Eng.
Academic Society:
- The Institute of Electrical Engineers of Japan

**Kenichi Ito**
Research Fields:
- Power Electronics Circuits
- Power Semiconductor Devices

Academic Societies:
- The Japan Society of Applied Physics
- The Institute of Electrical Engineers of Japan

**Yusuke Yamashita**
Research Field:
- Power Semiconductor Devices

Academic Society:
- The Japan Society of Applied Physics

Award:
- Technical Committee Encouragement Award on IEEJ Transactions on Electronics Information and Systems, The Institute of Electrical Engineers of Japan, 2015