Research Report

Reliability Design for Neutron Induced Single-event Burnout of IGBT

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ABSTRACT Single-event burnout (SEB) caused by cosmic ray neutrons leads to catastrophic failures in insulated gate bipolar transistors (IGBTs). It was found experimentally that the incident neutron induced SEB failure rate increases as a function of the applied collector voltage. Moreover, the failure rate increased sharply with an increase in the applied collector voltage when the voltage exceeded a certain threshold value (SEB cutoff voltage).

In this paper, transient device simulation results indicate that impact ionization at the n-drift/n^+ buffer boundary is a crucially important factor in the turning-on of the parasitic pnp transistor, and eventually latch-up of the parasitic thyristor causes SEB. In addition, the device parameter dependency of the SEB cutoff voltage was analytically derived from the latch-up condition of the parasitic thyristor. As a result, it was confirmed that reducing the current gain of the parasitic transistor, such as by increasing the n-drift region thickness d was effective in increasing the SEB cutoff voltage. Furthermore, 'white' neutron-irradiation experiments demonstrated that suppressing the inherent parasitic thyristor action leads to an improvement of the SEB cutoff voltage. It was confirmed that current gain optimization of the parasitic transistor is a crucial factor for establishing highly reliable design against chance failures.

KEYWORDS Single-event Burnout (SEB) of IGBT, White Neutron-irradiation, Parasitic Thyristor Action, Base Push-out Effect

1. Introduction

High-energy particles at sea level are produced in nuclear cascade showers created by nuclear spallation reactions between cosmic rays and atmospheric nuclei. There is general agreement that the flux of these particles is more than 97% neutrons at sea level.[1]

It has been reported that cosmic-ray neutrons cause probabilistic failures of power semiconductor devices.[2,3] The widely accepted failure mechanism is assumed to be as follows. Recoil ions produced by nuclear spallation reactions between incident neutrons and silicon nuclei form highly localized electron-hole plasma. The flow of generated charge distribution leads ultimately to localized breakdown of the semiconductor device.

Various analytical and numerical simulation models have been developed to analyze SEB of power metal-oxide-semiconductor field effect transistors (MOSFETs).[4-6] These papers show that turning-on of the inherent parasitic bipolar transistor in the device leads to highly localized current flow when the recoil ions strike power MOSFETs in the off state. The current-induced avalanche (CIA) caused by the transient current can trigger a second breakdown of the parasitic bipolar transistor, and neutron induced SEB eventually occurs.

In contrast, there have been few reports about SEB of IGBTs. The research described in this paper investigated SEB of IGBTs in hybrid electric vehicles (HEVs) using both transient device simulation and 'white' neutron-irradiation experiments.

The simulation model describes the initial generated charge distribution caused by the incident recoil ions in an IGBT during forward blocking state and the subsequent transient phenomena. The results showed that the peak electric field strength shifts from the n-drift/p-body junction to the n-drift/n^+ buffer boundary (nn^+ boundary) due to highly localized current in the IGBT. Therefore, the electric potential distribution is changed to a funnel-like shape. It was clarified that the onset of impact ionization at the nn^+ boundary

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can trigger turning-on of the inherent parasitic pnp transistor, consequently causing the SEB.

'White' neutron-irradiation experiments were also performed. The results obtained in this study indicated that the SEB failure rate of an IGBT increases sharply with an increase in the applied collector voltage when the voltage exceeds a certain threshold value. Moreover, it was observed for the first time that the aluminum electrode, which melted due to highly localized current, penetrated into the silicon, consequently forming an aluminum dendrite structure. The axially symmetric destruction traces probably show evidence that the SEB is an electrical destruction, not a mechanical destruction caused by the impact of nuclear spallation reactions between incident neutrons and silicon nuclei.

Furthermore, the 'white' neutron-irradiation experiments demonstrated that suppressing the inherent parasitic thyristor action increases the cutoff voltage for SEB failures. Current gain optimization of the parasitic transistor is a crucial criterion of device design for establishing highly reliable design against chance failures.

2. White Neutron-irradiation Experiments in Forward Blocking State

This research focused on the neutrons in terrestrial cosmic rays, which cause catastrophic failure of IGBTs because of their strongly penetrating radiation. High-energy neutron fluxes consist of 10 particles/cm^2/h at sea level and some 10^3 particles/cm^2/h at a typical airplane flight altitude of 30000 feet.(7)

The 'white' neutron beams were provided by the Los Alamos Neutron Science Center (LANSCE) and the Research Center for Nuclear Physics (RCNP) at Osaka University. The maximum energies of the beams were 750 MeV and 400 MeV, respectively. The 'white' neutron-irradiation experiments were performed at these facilities to investigate the SEB failure rate of IGBTs as a function of applied collector voltage.

The schematic of the experimental test circuit is shown in **Fig. 1**. The device was kept in the off state and DC collector voltage was applied during the 'white' neutron-irradiation. An oscilloscope measured the difference in potential between the two ends of the 10 Ω resistor to detect the SEB current of the DUT. A 10 kΩ current-limiting resistor was attached between the collector electrode and DC power supply.

The 'white' neutron-irradiation experiment showed that the failure rate of the IGBT increases sharply with an increase in the applied collector voltage when the voltage exceeds a certain threshold value (**Fig. 2**). In other words, the chip failure rate has a cutoff at lower applied voltage value. This characteristic cutoff is causally related to the latch-up destruction mode, which is discussed in the next section.

Moreover, a cross sectional scanning electron microscope (SEM) view of the destruction traces caused by neutron induced SEB was also observed (**Fig. 3** and **Fig. 4**). The SEM images show that the melting silicon in the n-drift region rapidly solidified and that a crack was generated due to contraction stress during the rapid cooling process. The destruction trace is an axially symmetric structure perpendicular

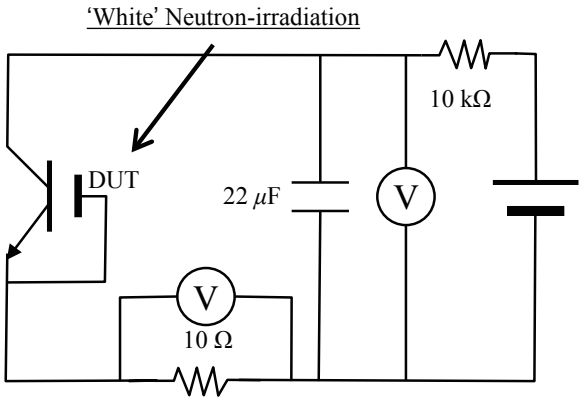


Fig. 1 Schematic of the experimental test circuit.

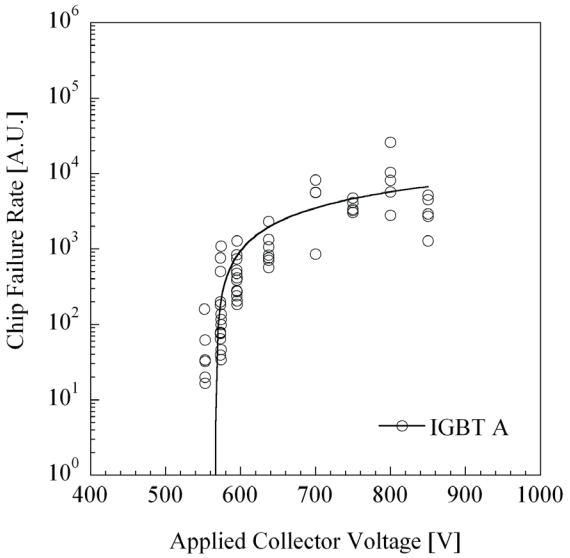


Fig. 2 SEB failure rate of IGBT type A as a function of applied collector voltage.

to the device surface and not in a random direction. An aluminum dendrite structure in the n-drift region was observed for the first time by element mapping using an energy dispersive X-ray (EDX) spectrometer (**Fig. 5**). The aluminum along the small grain boundaries of the silicon formed a dendrite structure. These results show evidence that the aluminum of the emitter-electrode penetrated into the silicon by electromigration, and the molten silicon region caused by the high current was rapidly cooled.

In addition, the size of molten silicon region depends on the capacitance value shown in Fig.1. This is because the capacitor discharge current flowed into the device after SEB occurred. That is, device failure has already been decided before silicon was melted due to highly localized current. Therefore, it is important to analyze triggering mechanism of the local short between collector and emitter, in order to clarify the root cause of SEB.

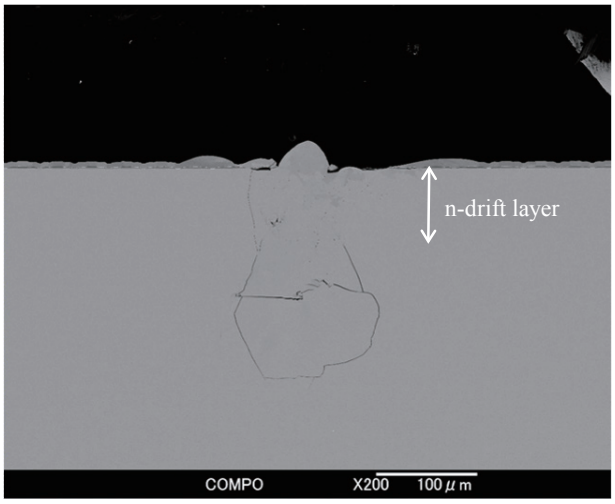


Fig. 3 Cross sectional SEM view of destruction trace caused by neutron induced SEB.

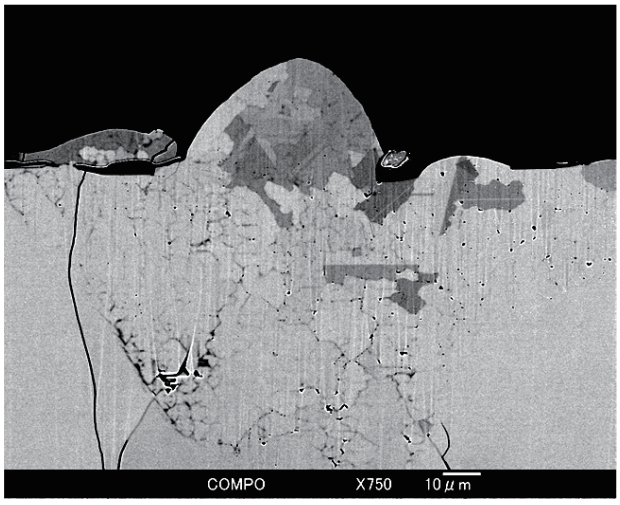


Fig. 4 Magnified SEM view of same image in Fig. 3.

3. Transient Device Simulation Analysis of Single-event Burnout

3. 1 Triggering Process of Single-event Burnout Caused by Inherent Parasitic Transistor Action

This section analyzes the triggering mechanisms for the SEB caused by the generated electron-hole pairs in an IGBT during forward blocking state, using commercial software DESSIS. The transient device simulations described the initial generated charge distribution along the ion track in the device. The recoil ions created by nuclear spallation reactions between incident neutrons and silicon nuclei lose the kinetic energy during travelling through the device. The lost energy is converted into generating electron-hole pairs along the track. In addition, the peak of generated electron-hole pairs occurs immediately before the recoil ion comes to rest.

Therefore, the spatial and temporal distribution of the generated charge was expressed as a Gaussian in the simulation model. The simulation model in this section also did not include the self-heating effect in order to analyze the electrical aspect of SEB. The

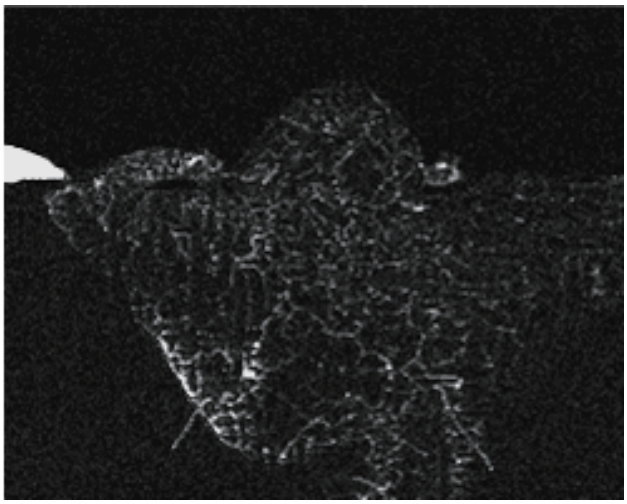


Fig. 5 Aluminum element mapping with energy dispersive X-ray (EDX) spectrometer in Fig. 4.

simulation used dimensions greater than the carrier diffusion length at room temperature. In this case, the width of IGBT is 132 μm (**Fig. 6**).

Figure 7 shows the applied voltage dependency of the collector current. A high collector current flows at a high applied collector voltage, which means that the IGBT is susceptible to destruction under high applied voltages. This simulation result provides certain evidence to support the experimental result of the SEB failure rate as a function of the applied collector voltage, as shown in Fig. 2.

The triggering process of SEB is discussed in detail below. The first current peak indicates that the initially generated charge carriers along the ion track are accelerated by the electric field in the depletion region at time (2) in Fig. 7 (1.3e-12 sec).

At time (3) in Fig. 7 and **Fig. 8** (3e-12 sec), the peak electric field strength shifts from the n-drift/p-body junction to the n-drift/n^+ buffer boundary (nn^+ boundary). This is the base push-out effect (Kirk effect) due to the highly localized current in the IGBT. Therefore, the electric potential distribution is changed to a funnel-like shape and, consequently carriers are generated at the nn^+ boundary due to the impact ionization (**Fig. 9** (a) and (b)). Injection of the generated carriers into the base neutral region triggers the turning-on of the inherent parasitic pnp transistor (p-body/n-drift/p^+ collector). Consequently, the hole carriers are injected into the n-drift region from the backside of the device (Fig. 9 (c) and (d)). These transient device simulation results indicate that the impact ionization at the n-drift/n^+ buffer boundary is important in the turning-on of the parasitic pnp transistor.

The critical current $I_{critical}$ for the base push-out is given by:

$$I_{critical} = qv_s\left[N_D + \frac{2\varepsilon_S\varepsilon_0 V_{cb}}{qd^2}\right]\cdot S, \quad (1)$$

where q is the elementary charge, v_s is the saturation

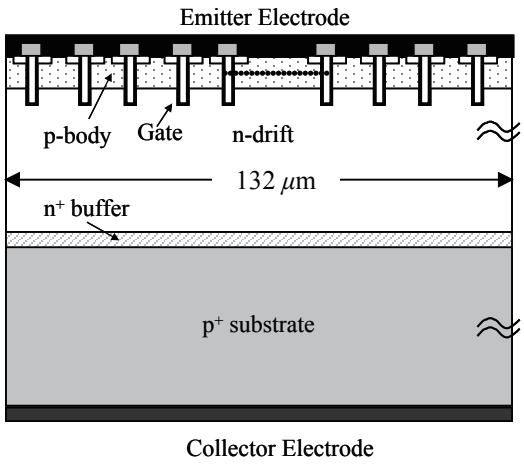


Fig. 6 Schematic cross-sectional view of the simulated IGBT.

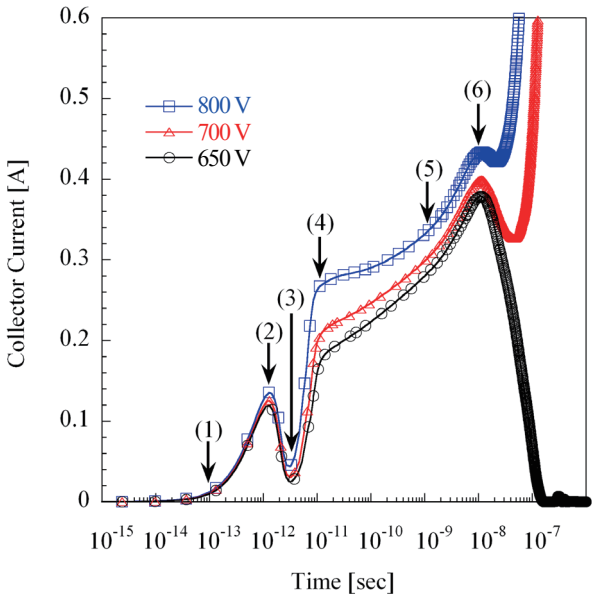


Fig. 7 Applied collector voltage (V_{ce}) dependency of collector current.

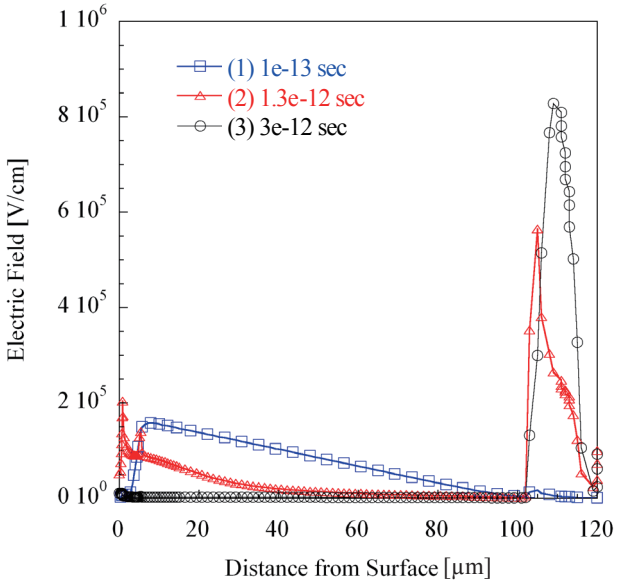
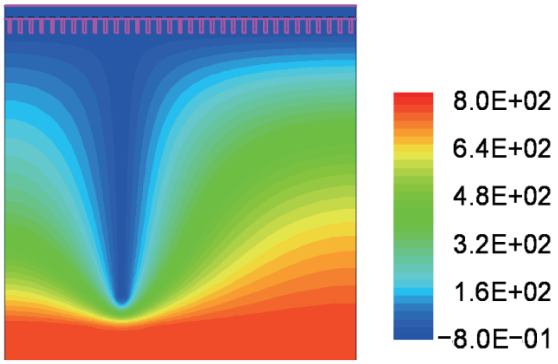
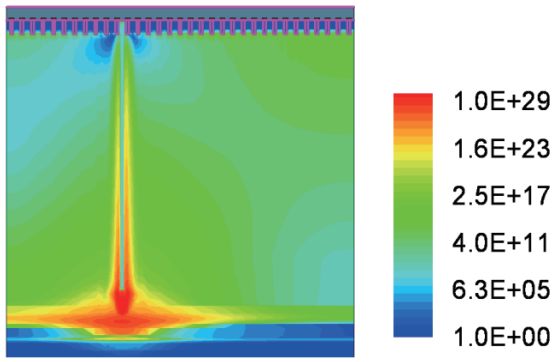


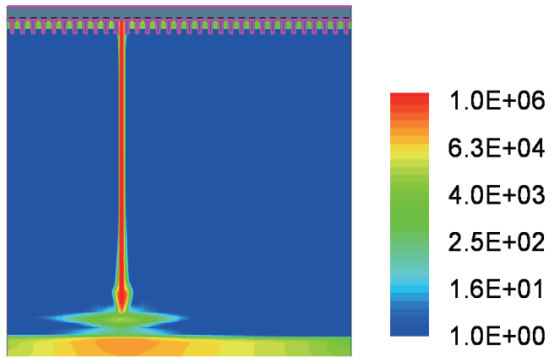
Fig. 8 Electric field distribution along ion track at the times shown in Fig. 7.



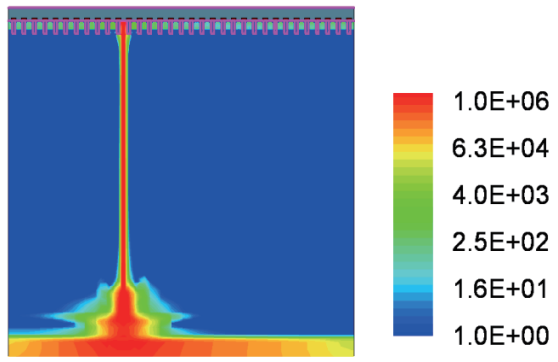
(a) Electrostatic potential [V] at time (3) 3e-12



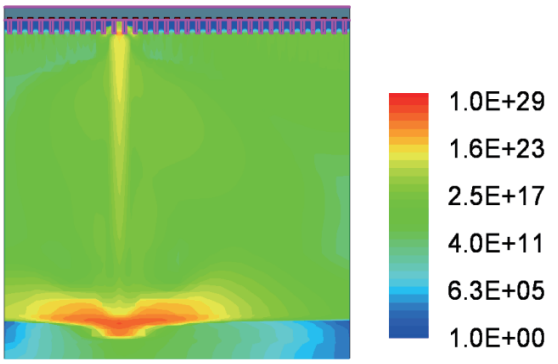
(b) Impact ionization rate [s^{-1} cm^{-3}] at time (3) 3e-12



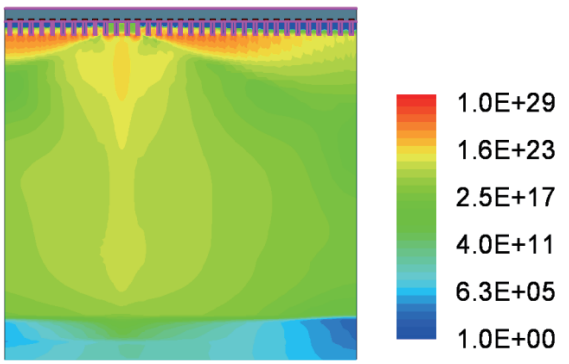
(c) Hole current density [Acm^{-2}] at time (3) 3e-12



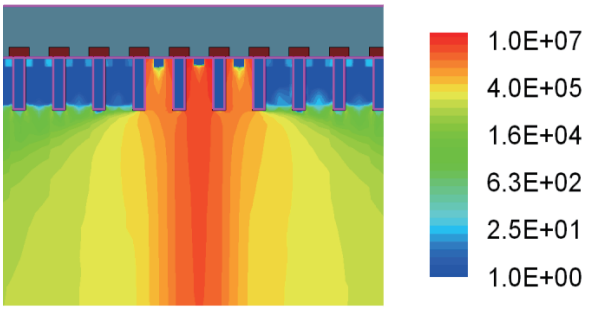
(d) Hole current density [Acm^{-2}] at time (4) 1.2e-11



(e) Impact ionization rate [s^{-1} cm^{-3}] at time (5) 1e-9



(f) Impact ionization rate [s^{-1} cm^{-3}] at time (6) 1.06e-8



(g) Electron current density [Acm^{-2}] at time (6) 1.06e-8.

Fig. 9 Simulated results of SEB at the times shown in Fig. 7.

velocity, N_D is the doping concentration of the n-drift region, d is the n-drift region thickness, ε_0 and ε_S are the permittivities of vacuum and Si, V_{cb} is the collector-base voltage of the inherent parasitic pnp transistor, and S is the cross sectional area of the SEB current flow. Therefore, the triggering charge density of the parasitic pnp transistor $N_{trigger}$ can be written as follows:

$$N_{trriger} \geq \frac{I_{critical}}{qv_S S} = \left(N_D + \frac{2\varepsilon_0 \varepsilon_S V_{cb}}{qd^2} \right). \quad (2)$$

This charge density $N_{trigger}$ consists of the initially generated carriers along the ion track and generated carriers due to impact ionization at the nn^+ boundary caused by the base push-out effect.

Figure 10 compares the simulated SEB current with and without the impact ionization model. The inherent parasitic pnp transistor did not turn-on in the case of the simulation without the impact ionization model. These simulation results indicate that impact ionization at the nn^+ boundary is crucially important to the turning-on of the inherent parasitic pnp transistor.

At the second current peak at time (6) in Fig. 7 (1.06e-8 sec), the inherent parasitic npn transistor (n^+ emitter/p-body/n-drift) turns on, and electrons are subsequently injected into the n-drift region (Fig. 9 (g)). Therefore, the electric field strength at the nn^+ boundary decreases due to the electron injection at this time. The lowering of the electrical potential between the p-body and n^+ emitter junction due to the electron injection leads to a temporary decrease in the collector current. Ultimately, the latch up of the parasitic thyristor action results in positive feedback of the collector current and, consequently, device destruction.

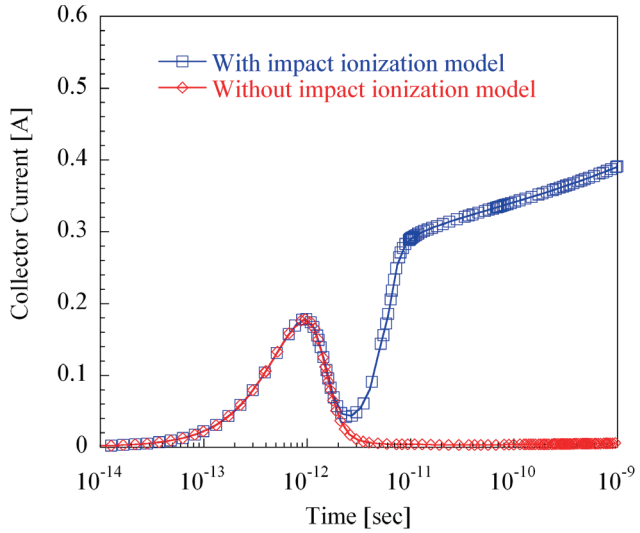


Fig. 10 Comparison of simulated SEB current with and without the impact ionization model.

From the results of the simulation analysis, it was concluded that the device has a propensity to destruct as the applied collector voltage rises because the current gain of the parasitic transistor increases due to the decrease in the neutral base width.

3. 2 Coupled Electro-thermal Simulations of Single-event Burnout

To calculate the temperature distribution in the device, the self-heating effect was modeled by incorporating a thermal diffusion equation. The maximum lattice temperature within the device increases with time, and the temperature ultimately reaches the melting point of silicon shown in **Fig. 11**. The temperature is locally distributed along the recoil ion track in the n-drift region in **Fig. 12**. The temperature profile shows a bimodal distribution, the shape of which reflects the profile of the electric field (**Fig. 13**). In particular, the temperature peak at the nn^+ boundary is attributable to the peak electric field caused by the base-push out effect.

The intrinsic carrier density also increases with the rising temperature for exactly the same reason (see **Fig. 14**). A rapid increase in intrinsic carrier density leads to a decrease in collector current because of the decrease in the current gain of the parasitic pnp transistor. Moreover, impact ionization has a negative temperature dependency. Therefore, the simulated collector current in the thermal model is low in comparison with the current in the isothermal model.

3. 3 Device Parameter Dependency of Cutoff Voltage for Single-event Burnout of Latch-up Mode

The chip failure rate has a cutoff within less than the certain voltage for SEB failures. Therefore, the SEB cutoff voltage is the most crucial parameter for high-reliability power device design. In this section, the device parameter dependence such as the thickness and the doping concentration of the n-drift region on SEB cutoff voltage is analytically derived from the latch-up condition.

The latch-up condition of a parasitic thyristor is

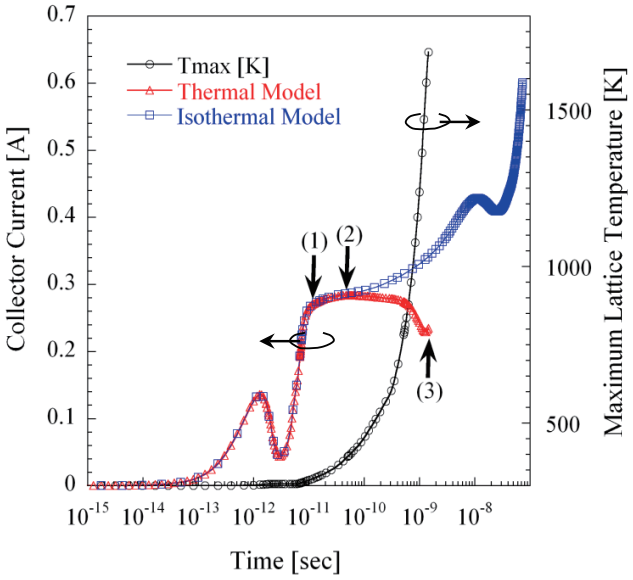


Fig. 11 Comparison of simulated SEB current between thermal and isothermal model, and maximum lattice temperature within the device.

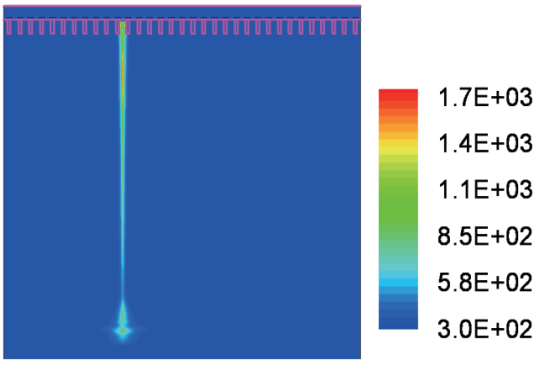


Fig. 12 Lattice temperature [K] distribution in n-drift region of IGBT at time (3) 1.5e-9 in Fig. 11.

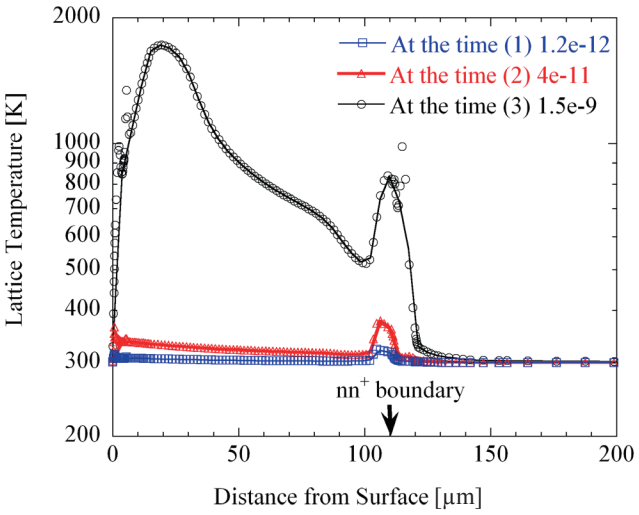


Fig. 13 Lattice temperature profile along the ion track at the times in Fig. 11.

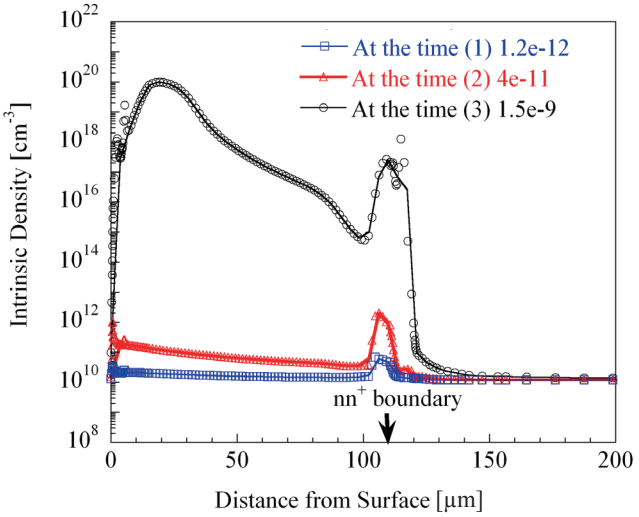


Fig. 14 Intrinsic density profile along the ion track at the times in Fig. 11.

given by the following equations.

$$\alpha_{pnp} + \alpha_{npn} \geq 1 , \tag{3}$$

$$\alpha_{PNP} = \frac{1}{\cosh\left(\frac{W}{L_a}\right)} \cong 1 - \frac{W^2}{2{L_a}^2} , \tag{4}$$

$$W \equiv d - \sqrt{\frac{2\varepsilon_0 \varepsilon_S V_{ce}}{qN_{eff}}} , \tag{5}$$

where α_{pnp} and α_{npn} are the base transport factors of the parasitic pnp and npn transistors, L_a is the ambipolar diffusion length in the n-drift region, W is the undepleted base width, N_{eff} is the effective space charge of the n-drift region, and V_{ce} is the applied collector voltage of the IGBT. The value of α_{pnp} is large at high V_{ce} values.

The applied collector voltage that triggers latch-up is obtained from Eqs. (3)-(5). The result is as follows:

$$V_{ce} \geq \frac{qN_{eff}}{2\varepsilon_0 \varepsilon_s}\left(d - L_a\sqrt{2\alpha_{npn}}\right)^2 = V_{SEB} , \tag{6}$$

where V_{SEB} is the cutoff voltage for SEB failures.

A decrease in α_{npn} has an effect on the improvement

of the cutoff voltage for SEB. It can be accomplished by an increase in p-body doping density and the depth. However, the increase in p-body doping density causes an increase in threshold voltage, and the depth is limited to less than the trench gate depth of IGBT. For the above reason, the increase in n-drift thickness is effective way to improve the cutoff voltage for SEB. It was experimentally demonstrated that the cutoff voltage increases with the increasing n-drift region thickness as shown in **Fig. 15**. This experimental result is in good agreement with Eq. (6).

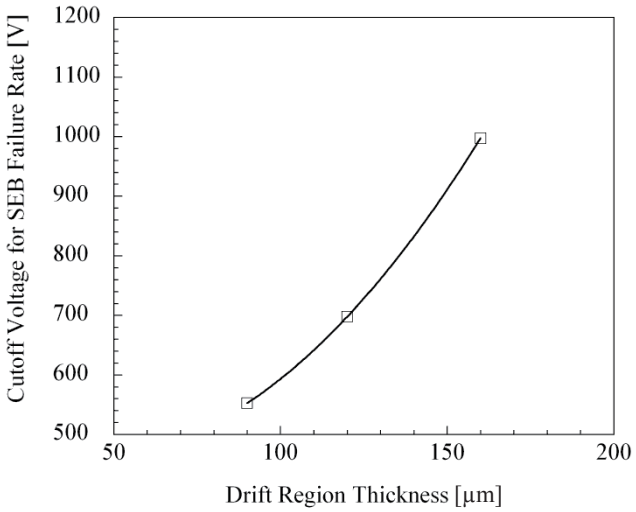


Fig. 15 Drift region thickness dependency of cutoff voltage for SEB failure rate.

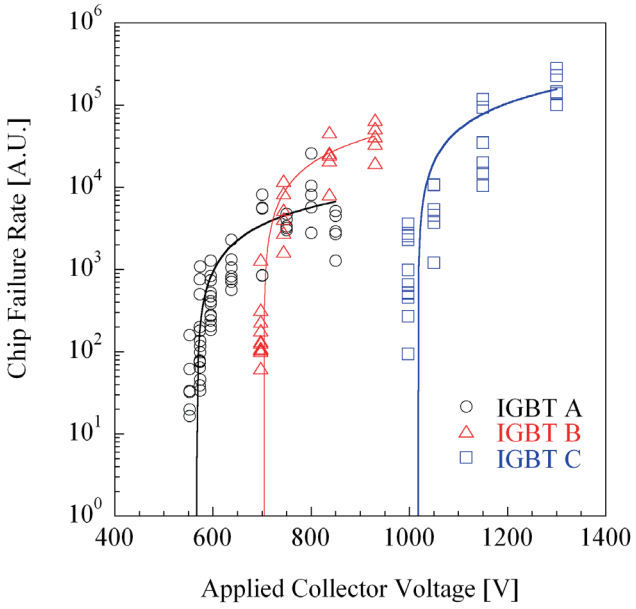


Fig. 16 SEB failure rate as function of applied collector voltage in IGBTs. (n-drift thickness *d*; IGBT C > IGBT B > IGBT A)

In this section, it was analytically confirmed that an effective way to increase the cutoff voltage for SEB failures is to reduce the current gain of the parasitic transistor, such as by increasing the n-drift region thickness *d*. Moreover, latch-up can never occur within less than V_{SEB} in Eq. (6). This is a main cause of the cutoff in the SEB failure rate under a low applied-collector voltage as shown in Fig. 2. Therefore, current gain optimization of the parasitic transistor is a crucial factor for establishing highly reliable design against chance failures.

4. Improvement of Cutoff Voltage for SEB Failure Rate

It was experimentally demonstrated that suppressing the inherent parasitic thyristor action leads to an improvement of the cutoff voltage for SEB failures of the IGBTs shown in **Fig. 16**. The inherent parasitic thyristor action was suppressed by changing the n-drift thickness. The n-drift thickness of the IGBTs was increased in the following order: IGBT A, IGBT B, and IGBT C. The relationship between the cutoff voltage for SEB failure rate and n-drift thickness is in agreement with the theoretical derivation shown in Eq. (6). Therefore, the cutoff voltage for SEB failures can be controlled by optimizing device parameters such as n-drift thickness.

It was clarified that current gain optimization of the parasitic thyristor for voltage rating is a crucial criterion for establishing highly reliable device design against chance failures.

5. Conclusions

'White' neutron irradiation experiments clarified that the SEB failure rate of an IGBT increases sharply with increases in the applied collector voltage when the value exceeds the cutoff voltage for SEB failure rate.

A current induced avalanche is triggered by highly localized electron-hole plasma along the recoil ion track, which is produced by nuclear spallation reactions between incident neutrons and silicon nuclei. The SEB of IGBT can be attributed to latch up of the parasitic thyristor caused by onset of impact ionization at the n-drift/n^+ buffer boundary (nn^+ boundary).

It is almost impossible to shield the IGBTs from cosmic-ray neutrons, and this is an unrealistic solution for reducing chance failures.

In this paper, it was confirmed experimentally and theoretically that the cutoff voltage for SEB failure rate can be controlled by designing the gain of the parasitic transistor using n-drift thickness or the like. Gain optimization of the parasitic transistor is an effective design criterion for establishing highly reliable devices against chance failures.

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