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Research Report

Consideration of PDM and Power Decoupling Method in an Isolated Single-phase Matrix Converter for Battery Charger

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ABSTRACT This report provides an overview of a proposed circuit structure and control schemes for the on-board battery chargers in plug-in hybrid and electric vehicles. The proposed structure employs a matrix converter, which, in comparison to a conventional converter, does not require an electrolytic DC smoothing capacitor and therefore makes downsizing possible. A power decoupling method that employs a center-tapped high frequency transformer and a small inductor capacitor (LC) buffer to suppress the single-phase power fluctuation caused by the lack of a DC-link bus in the matrix converter. Furthermore, the matrix converter applies pulse density modulation which can achieve zero-voltage switching to reduce the switching loss while controlling a 50 Hz/60 Hz sinusoidal waveform on the grid side. Harmonic analysis shows that the power decoupling method reduced the battery current ripple by 77.1% in comparison to the case without power decoupling. The experimental results also demonstrated that a clear sinusoidal waveform is obtained on the grid side with the proposed control scheme.

KEYWORDS Matrix Converter, Isolated Converter, Single-phase, Power Decoupling, Pulse Density Modulation

1. Introduction

An increasing focus on the reduction of CO_2 has led to a rapidly expanding growth of plug-in hybrid vehicles and electric vehicles. In order to sustain such growth, a small size, high efficiency and bidirectional energy controlled on-board vehicle battery charger is actively being researched.[1-2] **Figure 1** shows the power system architecture of an EV. In order to charge the high voltage battery, an isolated single-phase AC to DC converter is employed between the 50 Hz/60 Hz single-phase grid and the high voltage battery. The circuit structure for the battery charger is generally constructed with an AC/DC/AC converter as a primary converter, a high frequency transformer, and a secondary converter comprising an AC/DC rectifier.[3] In order to reduce the power ripple component in the battery current, which is caused by the single-phase grid power, bulky DC-link smoothing capacitors are required in the primary converter to absorb the fluctuation, which makes it difficult to downsize the battery charger.

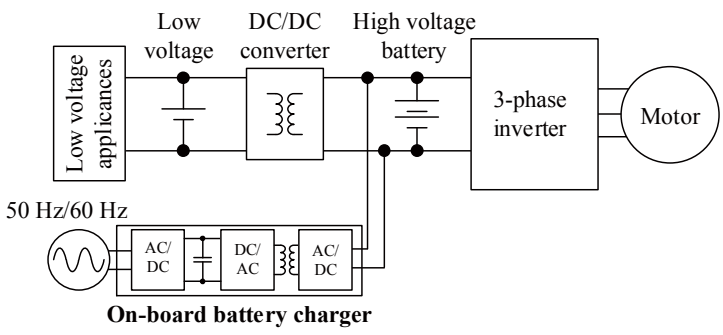


Fig. 1 Power system architecture of EV.

Many studies have shown that matrix converters promise a higher efficiency, a smaller size and a longer life-time than inverter-based circuits because DC-link smoothing capacitors are not needed.[4-6] A matrix converter performs a direct AC/AC conversion using only bi-directional switching devices and logic controls, therefore a DC-link bus is not formed in the circuit. As a result, the DC-link smoothing capacitor can be removed which provides a great advantage in term of sizing. This paper presents a circuit structure that applies the topology of a matrix converter between a single-phase grid and an isolated high frequency transformer instead of the conventional diode bridge rectifier and inverter (AC/DC/AC converter). However, due to the lack of a DC-link bus in the matrix converter, the power

ripple component in the battery current cannot be absorbed in single-phase grid.

In order to reduce power ripples in the battery current, the proposed structure uses power decoupling. Several circuit topologies with power decoupling methods have been studied.[7-12] These methods usually consist of a small buffer capacitor, a reactor, and a DC chopper to function as an energy buffer to absorb the power fluctuation. However, these circuits struggle to achieve high efficiency because as a tradeoff for the passive components, more switching devices are used. One method adds current loop control, which reduces the ripple current in the existing voltage loop control system without additional converters or energy storage components for power decoupling.[7] However, to sustain the voltage level at the DC-link bus, there is a tradeoff between current loop and voltage loop controls. As a result, the DC-link smoothing capacitor has to be large enough to also control the voltage loop and therefore the size of the capacitor cannot be reduced significantly, even with the application of power decoupling. However, one approach to power decoupling utilizes a center-tapped transformer with a small inductor capacitor (LC) buffer in a full bridge inverter.[13] This topology can compensate for the power fluctuation without adding extra switching devices, because the existing switching devices in the full bridge inverter can be utilized to perform the power decoupling.

This paper presents the circuit structure for a matrix converter with a center-tapped transformer. The size and weight of the on-board battery charger can be greatly reduced because it uses only a small LC buffer circuit to achieve power decoupling in the battery current, and use of the matrix converter in the primary converter removes the bulky DC-link smoothing capacitor.

This paper also presents an overview of the proposed control scheme. The control method for matrix converter is pulse density modulation (PDM) based on pulse width modulation (PWM),[14-15] and the control method for the secondary converter (inverter) is carrier comparison-based PWM. This control method can reduce the conversion loss because it enables zero-voltage switching (ZVS) by synchronizing the gate pulses of the matrix converter with the zero-voltage term of the transformer voltage. First, the circuit topologies are compared and discussed, and then the proposed control scheme is explained accordingly. Finally, the validity of the control scheme for the proposed circuit is evaluated experimentally.

2. Circuit Topology

2. 1 Conventional Converters

Figure 2 shows a conventional isolated DC to single-phase AC converter. The conventional circuit comprises a full bridge inverter, a high frequency transformer and an AC/DC/AC rectifier-inverter. The full bridge inverter outputs a square-wave voltage at a high frequency to reduce the size of the transformer. The secondary rectifier converts the high frequency voltage to a DC voltage, and the PWM inverter controls the grid current using feedback control.

When the load current has a sinusoidal waveform and unity power factor, the instantaneous output power p_{out} is expressed by Eq. (1).

$$\begin{aligned} p_{\mathrm{out}} &= \sqrt{2}V_{\mathrm{grid}}\sin(\omega_{\mathrm{o}}t)\cdot\sqrt{2}I_{\mathrm{grid}}\sin(\omega_{\mathrm{o}}t) \\ &= V_{\mathrm{grid}}I_{\mathrm{grid}}\{1-\cos(2\omega_{\mathrm{o}}t)\} = P_{\mathrm{out}}\{1-\cos(2\omega_{\mathrm{o}}t)\}, \end{aligned} \tag{1}$$

where, V_{grid} is the grid voltage (RMS), I_{grid} is the grid current (RMS), P_{out} is the output mean power and ω_{o} is the output angular frequency. The ripple component expressed by the second term in Eq. (1) should be bypassed in order to obtain a constant DC current in the DC-link bus. Hence, this system must use a bulky electrolytic capacitor C_{dc} and an inductor L_{dc} to absorb this power ripple.

Figure 3 shows an isolated DC to single-phase AC converter with a DC active buffer circuit.[13] This circuit comprises a full bridge inverter, a high frequency center-tapped transformer, a small LC buffer circuit and an AC/DC/AC rectifier-inverter. The full bridge inverter and LC buffer circuit

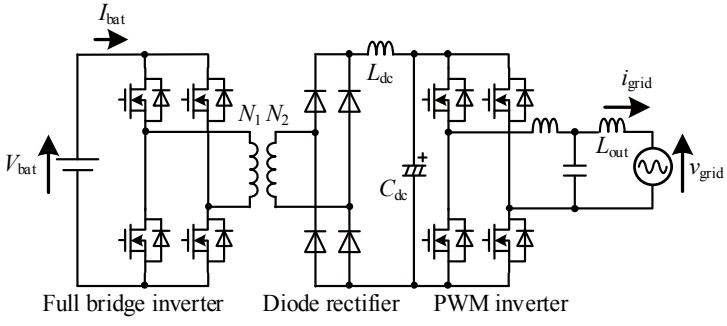


Fig. 2 Conventional isolated DC to single-phase AC converter.

function as a DC active filter using the center-tapped transformer. Therefore, the inverter has capabilities of both a full bridge inverter and a buffer circuit. This circuit structure does not require additional switching devices, unlike a conventional power decoupling circuit. However, the circuit still needs a large DC-link smoothing capacitor C_{dc} to transfer power to the transformer because this system involves an isolated DC to single-phase AC converter using a AC/DC/AC rectifier-inverter.

2. 2 Proposed Converter

Figure 4 shows the isolated DC to single-phase AC converter using the matrix converter and small *LC* buffer which is proposed in this paper. The matrix converter is employed in order to eliminate the DC-link smoothing capacitor C_{dc}, which is shown in Fig. 2. Direct AC/AC conversion between the isolated transformer and the single-phase grid can then be achieved. The center-tapped transformer links the full bridge inverter to the matrix converter for isolation and also performs power decoupling that reduces the power ripple in the battery current. The buffer circuit includes a buffer capacitor C_{buf} and a buffer inductor L_{buf}. Charging and discharging the buffer capacitor

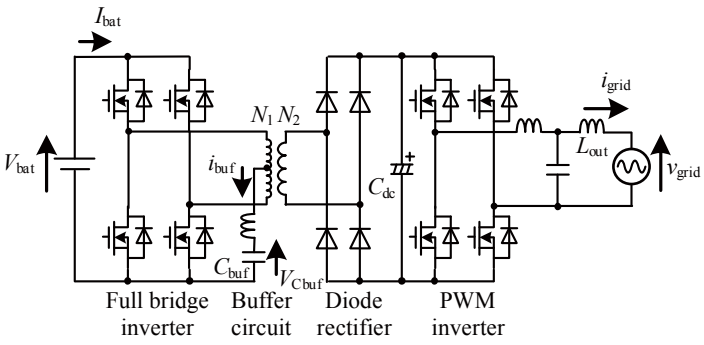


Fig. 3 Isolated DC to single-phase AC converter with LC buffer circuit.

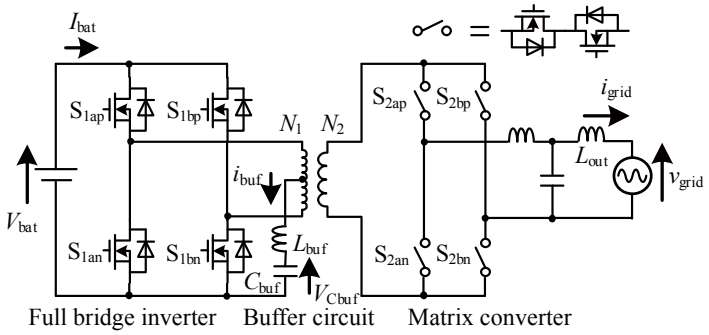


Fig. 4 Proposed isolated DC to single-phase AC converter.

C_{buf} compensates for the power ripple. In addition, the switching loss in the matrix converter can be reduced because ZVS is enabled by synchronizing the gate pulses of the matrix converter with the zero-voltage term of the transformer voltage. As a result, the proposed converter achieves a higher efficiency, a smaller size and a longer life-time than conventional rectifier-inverter structures.

Figure 5 shows the principle of the power decoupling method with C_{buf}. The relationship among the output power p_{out}, the battery power P_{bat} and the buffer power p_{buf} is given by

$$p_{out} = P_{bat} - p_{buf}\,, \tag{2}$$

$$p_{out} = P_{bat}\,, \tag{3}$$

$$p_{buf} = P_{out}\cos\left(2\omega_o t\right), \tag{4}$$

where the polarity of p_{buf} is defined as positive when C_{buf} is charged. In order to smooth the battery current, the buffer circuit has to reduce the ripple component in Eq. (1). Therefore, p_{buf} is equivalent to the second term of Eq. (1). It should be noted that the capacitor used here is smaller than that for the conventional converter because power ripple compensation is accomplished by varying the voltage across the buffer capacitor v_{Cbuf} and not the capacitance. On the other hand, the inductor in the buffer circuit is used for current control for power decoupling, which is equivalent to controlling p_{buf}. The buffer current is controlled by the full bridge inverter, which outputs a differential mode voltage to excite the transformer and a common mode voltage to compensate for the power ripple with the LC buffer independently, owing to the center-tapped transformer. Thus, the proposed converter does not require additional switching devices for power decoupling, and the number of devices in the proposed converter and a conventional circuit is the same, which reduces the cost.

3. Control Strategy

Figure 6 shows a control block diagram for the proposed circuit structure. The current and voltage controls in the proposed converter are implemented by proportional-integral (PI) controllers. The full bridge inverter independently provides a differential mode voltage to excite the transformer and a common mode voltage to compensate for the power ripple.

Buffer current control is applied to vary the voltage across the buffer capacitor v_{Cbuf} and absorb the power ripple. Modulation of the matrix converter is discussed in Sec. 4.

First, the buffer capacitor energy W_{Cbuf} is obtained using Eq. (5) and the voltage-current equation for the capacitor.

$$W_{\mathrm{Cbuf}} = \int_{t_0}^{t} v_{\mathrm{Cbuf}} i_{\mathrm{buf}} d\tau = \int_{t_0}^{t} v_{\mathrm{Cbuf}} \left(C_{\mathrm{buf}} \frac{dv_{\mathrm{Cbuf}}}{d\tau} \right) d\tau = \int_{t_0}^{t} P_{\mathrm{ave}} \cos(2\omega_{\mathrm{o}}\tau)\, d\tau, \quad (5)$$

where t_0 is the operation starting time. The buffer capacitor voltage v_{Cbuf} which is needed to absorb the

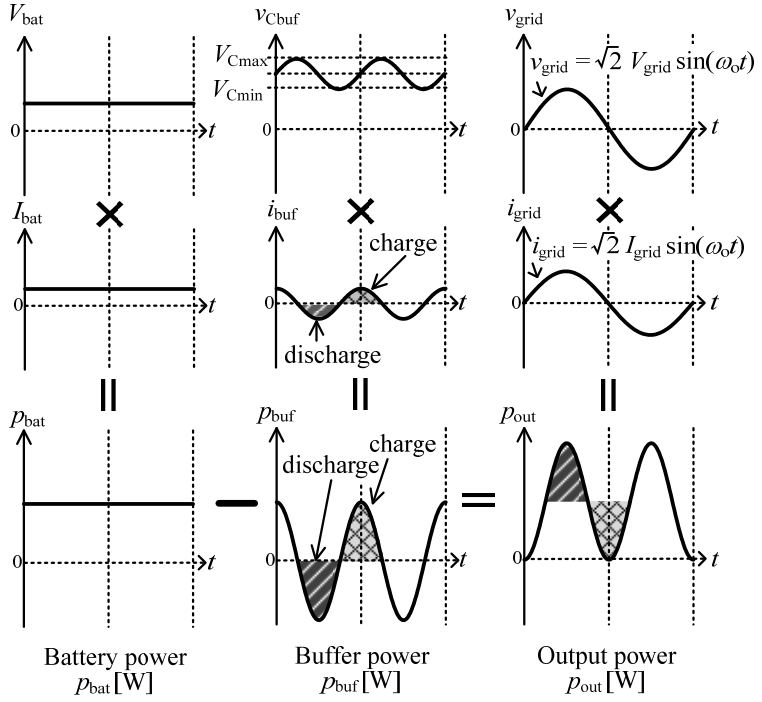


Fig. 5 Principle of power decoupling with buffer capacitor C_{buf} which is charged or discharged to compensate for the power ripple.

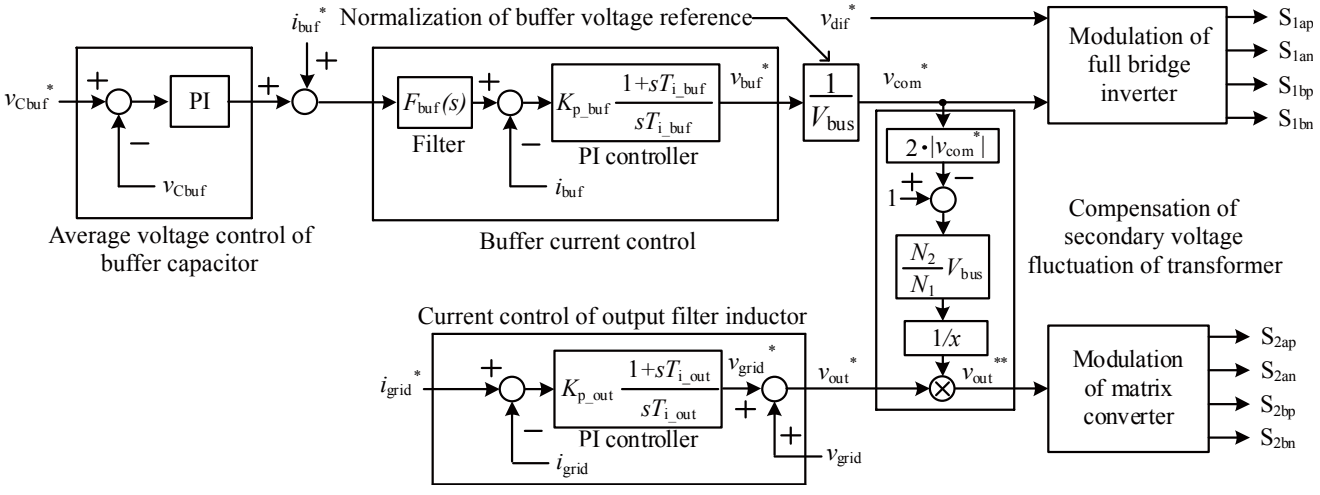


Fig. 6 Control block diagram for the proposed converter. Buffer current control enables power decoupling. The output filter current control is applied as a minor loop of the output filter capacitor voltage control that is originally required.

power ripple is given by

$$v_{\mathrm{Cbuf}} = \sqrt{{V_{\mathrm{C0}}}^2 + \frac{P_{\mathrm{ave}}}{\omega_{\mathrm{o}} C_{\mathrm{buf}}}\left\{\sin(2\omega_{\mathrm{o}} t) - \sin(2\omega_{\mathrm{o}} t_0)\right\}}, \quad (6)$$

where V_{bat} is the average battery voltage and P_{ave}* is calculated from the load resistance. The buffer current i_{buf} is given by

$$i_{\mathrm{buf}}{}^{*} = C_{\mathrm{buf}} \frac{dv_{\mathrm{Cbuf}}{}^{*}}{dt} = \frac{P_{\mathrm{ave}}{}^{*} \cos(2\omega_0 t)}{\sqrt{\frac{{V_{\mathrm{bat}}}^2}{4} + \frac{P_{\mathrm{ave}}{}^{*}}{\omega_{\mathrm{o}} C_{\mathrm{buf}}} \sin(2\omega_{\mathrm{o}} t)}}. \quad (7)$$

The output filter current control is applied as a minor loop of the output filter capacitor voltage control that is originally required. The buffer capacitor voltage control is introduced in order to avoid divergence of the average voltage due to discretization.

4. Modulation Method of Matrix Converter

Figure 7 shows the PDM concept as applied in the matrix converter.[14-15] PDM treats the high frequency transformer voltage waveform as a pulse and synthesizes the output voltage (grid voltage) with the density of the transformer pulse voltage. In Fig. 7, a half cycle of the transformer pulse voltage is used as the minimum unit for the output voltage waveform. Note that, the control converts the full bridge inverter output to a three-level square waveform. As a result, by synchronizing the control of the matrix converter with the full bridge inverter, the switching interval in the matrix converter can be used to achieve ZVS and reduce the switching loss.

Figure 8 shows a block diagram of the PDM control based on PWM. First, the PDM method produces a PWM pulse, which is generated by triangular carrier comparison. In order to convert the PWM pulse to a PDM pulse, the PWM pulse is forcibly synchronized with the zero-voltage term of the transformer voltage by a D flip-flop. The PWM pulse is then synchronized with both edges of the primary switching signal S_{1bn} because these edges coincide with the zero-voltage term of the transformer voltage. In addition, the gate signal of the matrix converter is controlled according to the polarity of the transformer voltage through CLK and EXNORs.

Figure 9 shows the relationship between the output voltage reference v_{out}* and the output voltage waveform with the PDM, that is the result when v_{out}* changes from 0.20 to 0.25, and 0.30 p.u. The output voltage ripple is high because the PDM method outputs series of concentrated pulse voltage instead of distributed pulse voltages. Furthermore, when

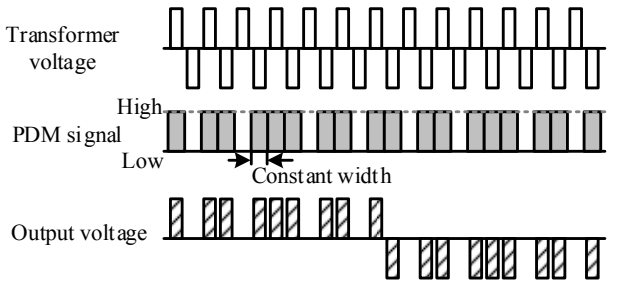


Fig. 7 PDM method applied in the matrix converter.

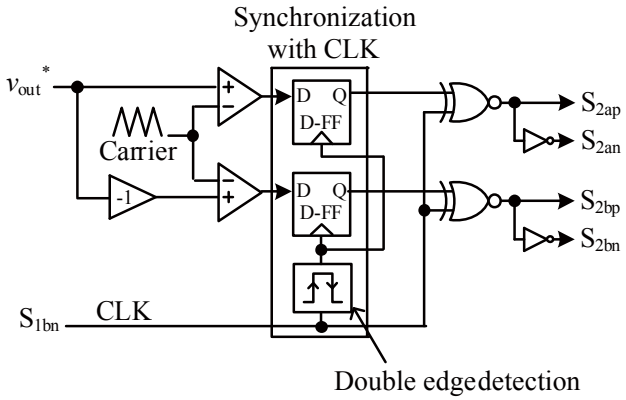


Fig. 8 Block diagram of PDM based on PWM.

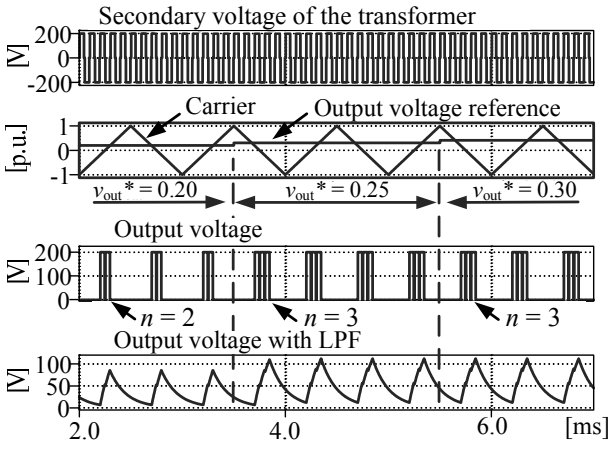


Fig. 9 Waveform of matrix converter with PDM based on PWM. The output voltage is in the form of concentrated pulses within one carrier period.

v_{out}* = 0.20 p.u., the output pulse number n within half the carrier period is 2. In contrast, when v_{out}* = 0.25 and 0.30 p.u., n is 3 within half the carrier period. As a result, n within half the carrier period is expressed by

$$n = \frac{f_{trans}}{f_{sw}} v_{out}^* , \quad (8)$$

where f_{trans} is the frequency of the transformer voltage and f_{sw} is the carrier frequency of the matrix converter. It should be noted that n is rounded to an integer because the PDM pulses exist only as integers. In Fig. 9, for simplicity f_{trans} and f_{sw} are set to 10 kHz and 1 kHz, respectively. This makes the carrier frequency ratio become 10. Thus, n becomes 2 while v_{out}* = 0.20 in half the carrier period. In contrast, n which should be 2.5 becomes 3 while v_{out}* = 0.25 in half the carrier period because the PDM method does not consider digits after the decimal point. This error is called the quantization error, and increases the output voltage distortion, and it is influenced by the resolution N_{res} of the PDM. Consequently, n is proportional to N_{res} which is expressed by Eq. (9). Also note that, v_{out}* is proportional to the modulation index α in the matrix converter.

$$N_{res} = \frac{f_{trans}}{f_{sw}} \alpha \quad (9)$$

If the output voltage reference is a sinusoidal waveform, the pulse density of the output voltage is changed stepwise by quantization. In addition, N_{res} is always an integer representing the pulse density.

From Eq. (9), if the carrier frequency ratio or α is lower, N_{res} for an output voltage waveform is lower. As a result, the distortion with respects to the fundamental component of the output voltage increases with the quantization error. Especially, if α is lower, the term in the generation of the quantization error becomes longer by decreasing dv/dt of v_{out}*. Moreover, if the carrier frequency ratio is small, the quantization error becomes higher due to a decrease in the pulse density. Thus, if the resolution N_{res} is lower, the quantization error becomes higher and the output voltage distortion increases. Furthermore, due to the PWM comparison method, high frequency transformer pulse voltage is converted to a low frequency concentrated pulse voltage at the output of the matrix converter, which increases the output voltage ripple. Therefore, a grid inductor (L_{out}) with larger inductance is required to improve the harmonic components of the output current.

5. Experimental Results

Table 1 shows the experimental parameters for the isolated single-phase matrix converter with PDM. It should be noted that the carrier frequency ratio is 10:1 and the output side is an R-L load without an LC filter.

5. 1 ZVS with PDM

Figure 10 shows the extended experimental waveform for PDM. The results show that the gate

Table 1 Experimental parameters.

DC bus voltage	350 V_{dc}	Load voltage	100 V_{peak}
Load frequency	50 Hz	Device rated voltage	650 V
Buffer L (L_{buf})	2.0 μH	Buffer C (C_{buf})	200 μF
Grid conneted inductor L (L_{out})	2.0 mH	Turn ratio of transformer N_2/N_1	1
Carrier frequency of full bridge inverter	100 kHz	Carrier frequency of matrix converter	10 kHz
Natural angular frequnecy of buffer current controller	4000 rad/s	Natural angular frequnecy of filter current controller	4000 rad/s
Damping factor of buffer current control	0.7	Damping factor of filter current control	0.7

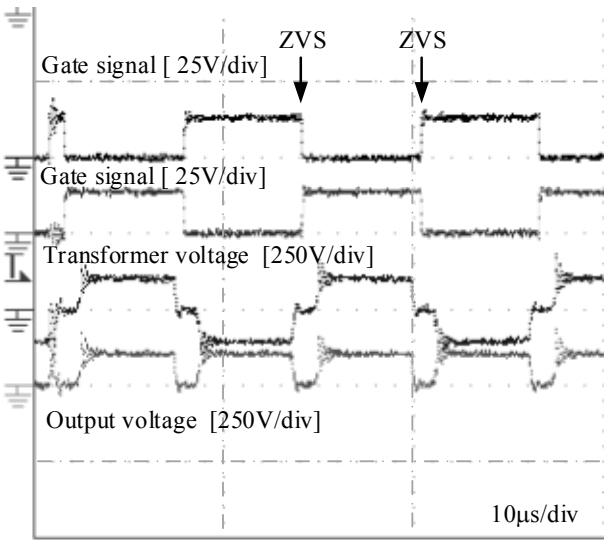


Fig. 10 Experimental waveforms for PDM in the matrix converter, which demonstrate ZVS behaviour.

signals from matrix converter achieve ZVS, where the switching intervals coincide with the zero-voltage term of the transformer voltage. In **Fig. 11**, the relationship for PDM based on PWM is shown, where the output voltage is in the form of a concentrated series based on the duty and carrier frequency ratio, as explained above.

5. 2 Power Decoupling with PDM Based on PWM

Figure 12 shows the experimental waveforms for the proposed converter, (a) without power decoupling and (b) with power decoupling, respectively. In Fig. 12(a), it is noted that the buffer capacitor voltage does not vary because decoupling control is deactivated. As a result, the buffer current is constant at zero and power ripples occur in the battery current. In contrast, Fig. 12(b) demonstrates that with the implementation of decoupling control, the power ripple component in the battery current is reduced, and the buffer current shows a sinusoidal waveform with a frequency twice of the output voltage frequency. This indicates that the buffer circuit that connects to the center-tapped transformer is operating to suppress power ripples in the battery current by the mechanism shown in Fig. 5. However, high-order distortion occurs in the battery current due to the effect of the quantization error in the output voltage, which is a result of the compensation reference, as expressed by Eq. (1), not coinciding with the actual power fluctuation, since the proposed power decoupling method is based on the premise that the power ripple is a sinusoidal waveform without distortion.

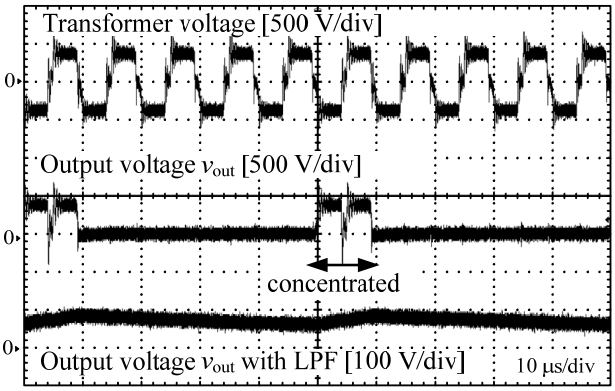
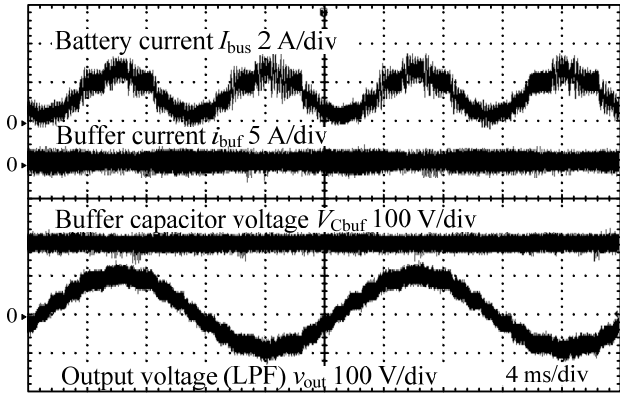


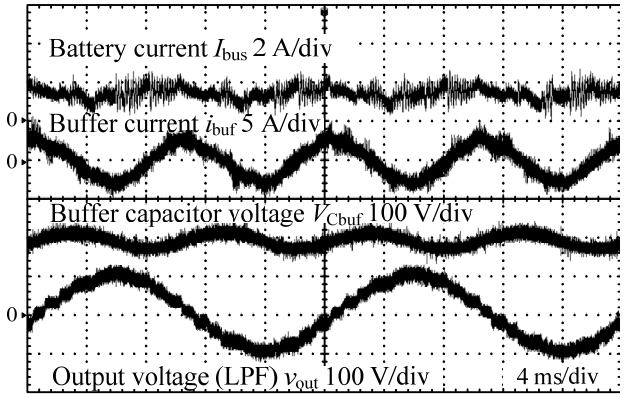
Fig. 11 Relationship between the output voltage and transformer voltage in PDM based on PWM.

5. 3 Harmonic Analysis

Figure 13 shows the results of harmonic analysis of the battery current. It should be noted that the harmonic number is based on an output frequency of 50 Hz. From the results without power decoupling, the power ripple component at 100 Hz was 57.4% with reference to the average battery current. On the other hand, the proposed power decoupling method with PDM reduced the 100 Hz component to 13.1%. However, the 100 Hz component of the power ripple in the battery current remained because of the quantization error and the output voltage ripple affecting the power ripple component. These experimental results verified the effectiveness of the proposed circuit and the control scheme with PDM.



(a) Without power decoupling



(b) With power decoupling

Fig. 12 Experimental waveforms with PDM based on PWM. The proposed power decoupling method provides the common mode AC voltage to drive fluctuations in the buffer capacitor voltage.

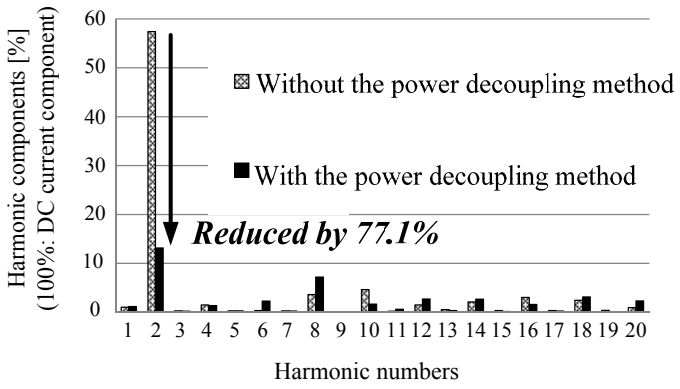


Fig. 13 Harmonic analysis of the battery current. The power decoupling method reduces the battery current ripple by 77.1% with the proposed voltage error compensation method.

6. Conclusion

This paper presented an overview of an isolated single-phase matrix converter with PDM and power decoupling. The proposed circuit structure is expected to be smaller than a conventional rectifier-inverter circuit because the bulky DC-link smoothing capacitor is not required. In addition, the effectiveness of power decoupling control utilizing a center-tapped transformer with a full bridge inverter was confirmed in the experiment. From the experimental results, the proposed power decoupling method can reduce the battery current ripple by 77.1%.

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