Special Feature: Power Electronics for Hybrid Vehicles

Research Report

Analysis of Common-mode Noise Generation Mechanism in FM Radio Band Caused by DC-DC Converter

Atsuhiro Takahashi, Hiroshi Tsukada, Takashi Kojima, Yoshiyuki Hattori, Tsuyoshi Funaki and Osami Wada

Report received on Feb. 14, 2017

ABSTRACT In this paper, generating mechanism of common-mode voltage at DC input of a full-bridge DC-DC converter is analyzed in FM-radio band. Transient noise voltage with dumped oscillation, generated by switching of the transistors, acts as a differential noise source, and it drives the common-mode voltage due to the lack of balance of impedances between two power lines. Even though the impedances of these lines are balanced, the total balance is lost due to the parasitic capacitances between the midpoints of upper and lower arms and the ground. Accordingly, the capacitances of the balanced circuit should be much larger than the parasitic capacitances to reduce the common-mode voltage.

KEYWORDS DC-DC Converter, Common-mode Current, Impedance Balance, Reduction of Noise

1. Introduction

Electric power converters are present in a wide variety of systems ranging from home electrical appliances to automobiles. In such converters, electromagnetic noise caused by the switching of transistors inside the circuit can interfere with the proper operation of other electronic components. For this reason, the suppression of such noise is important.

One form of electromagnetic interference to electronic devices by power converters is to reception of radio broadcasts. In recent years, the increasingly high switching frequencies of electric power converters has reduced the rise and fall times of switching circuits, ensuring that the effects they produce remain significant even at high-harmonic frequencies. Thus, interference is problematic not only for AM radio (0.5-1.6 MHz) but also for FM radio (76-108 MHz).

In many cases, this radio-frequency interference is caused by common-mode currents in electric power converters. Though the magnitude of the common-mode current is smaller than that of the normal-mode current, the electric field it radiates is larger.[1-2] Among the various types of electric power converters, the mechanisms responsible for common-mode currents have previously been analyzed for three-phase inverters,[3] but remain unclear for DC-DC converters (DDCs).

In this paper, we analyze the mechanisms responsible for the appearance of FM radio-frequency common-mode voltages in DDCs like those depicted schematically in **Fig. 1**. Our reasons for analyzing common-mode *voltages* instead of common-mode *currents* are explained below. This DDC, a voltage downconverter that inputs 200 V from a high-voltage battery and outputs a 14 V supply voltage to a load, is a standard component used in hybrid electric vehicles (HEVs). The circuit has two input terminals (positive

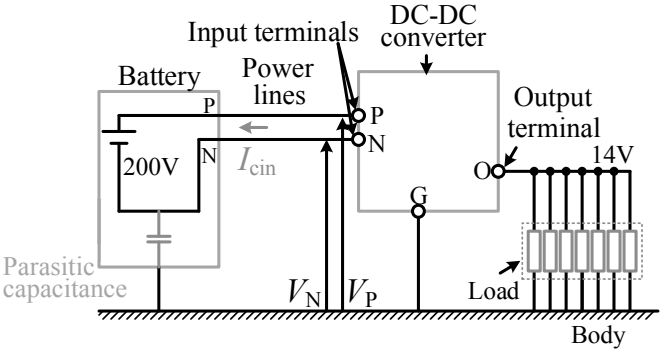


Fig. 1 DC-DC converter and its external conditions.

Reprinted from the original publication of IEICE Trans. B, Vol. J99-B, No. 3 (2016), pp. 144-154, (IEICE Transactions Online :http://search.ieice.org/index.html),

(P) and negative (N)) and two output terminals (output (O) and ground (G)).

We focus on the common-mode voltage at the input terminals, and analyze the mechanisms responsible for producing it. Our reasons for focusing on the input terminals are as follows: As shown in Fig. 1, the input terminals of the DDC are connected by wires to the positive and negative terminals of a high-voltage battery. These wires are insulated from the body to prevent electric shock.[4] The O output terminal of the DDC is connected to the 14 V battery and the load, while the G terminal is connected to the body. Taking the body as the ground reference for the common-mode component of signals, the common-mode impedance at the input of the DDC is several hundred ohms at FM radio frequencies, while the output impedance is a few ohms or less. Consequently, we expect that the dominant contribution to FM radio interference will come from electric fields radiated from the input side of the circuit, with its larger common-mode impedance. We therefore focus on the input terminals in this study.

We now explain our reasons for focusing on common-mode voltages instead of currents. As shown in Fig. 1, the common-mode current I_{cin} flowing into the input terminals of the DDC is the current flowing through the P and N power-supply lines in the same direction. Denoting the common-mode impedance of the input terminals with respect to the body by Z_{r} and the common-mode voltage by V_{cin}, the current I_{cin} may be expressed in the form

$$I_{\mathrm{cin}} = \frac{V_{\mathrm{cin}}}{Z_{\mathrm{r}}} . \tag{1}$$

Similarly, assuming the input terminals are driven by a balanced line input, V_{cin} is given by

$$V_{\mathrm{cin}} = \frac{V_{\mathrm{P}} + V_{\mathrm{N}}}{2} . \tag{2}$$

Here, V_{P} and V_{N} are the voltages arising between the P and N terminals and the body in Fig. 1. Equation (1) shows that I_{cin} depends on V_{cin}, and thus if V_{cin} can be zeroed out then there will be no current I_{cin}, regardless of the impedance of the wires connected to the terminals or the impedance of the battery. For these reasons, we focus on the common-mode voltage at the DDC input terminals, and analyze the mechanisms responsible for producing the voltage.

There have been several previous reports on techniques for predicting and suppressing common-mode voltages generated by DDCs.[5-11] Predictive methods include a quantitative technique in which conductive noise generated by the DDC in the VHF band (30-300 MHz) was analyzed numerically,[5] while suppression techniques include a method for optimizing the placement of Y-capacitors near the transistors that serve as noise sources[6] and a method based on the application of zero-voltage switching (ZVS).[7] Techniques for suppressing common-mode voltages at sub-FM-radio frequencies of 30 MHz and below include improving the impedance balance of the power-supply interconnect wires[8-10] and controlling the switching of transistors.[11]

An analysis of FM-radio-band common-mode voltages in CMOS microcontrollers has also been reported.[12] This study noted that fluctuations in the power-supply voltage (V_{d}) due to through-currents flowing from CMOS power-supply lines and ground lines serve as noise sources. The study also noted that the common-mode voltage V_{cin} is determined by V_{d} and by the balance of the impedances of the PCB power-supply and ground lines referred to the ground reference.

In this paper, we focus on electric power converters. In power converters, unlike CMOS circuits, dead time is designed into the switching of the semiconductor devices in the upper and lower arms to ensure that no through-currents arise. Moreover, for CMOS circuits, in which large numbers of semiconductor devices simultaneously turn on and off, the impedance between the ground reference and various interconnect lines, including power-supply and ground lines, may be properly taken into account using only its average value; variations with operating state may be ignored. In contrast, power converters have few semiconductor devices, and the switching behavior of each device is independent of the other devices, prohibiting the use of average quantities as is possible for CMOS circuits. For these reasons, it is believed that the quantities V_{d} and V_{cin} arise due to mechanisms different from those present in CMOS circuits. However, the generation mechanism for the noise remains unclear.

In this paper, we consider an idealized DDC and theoretically analyze the mechanisms responsible for voltage fluctuations V_{d} at FM-radio frequencies. We then show that the common-mode voltage V_{cin} at the input terminals arises due to impedance imbalances. Finally, we show that, in actual DDCs, a parasitic capacitance C_{s} is present between ground and the midpoint of the arm, and that this offsets the

impedance balance in the power-supply lines, thus influencing V_{cin}.

2. Circuit Topology and Operation of the DDC

In this section, we discuss the circuitry and operation of the DDC analyzed in this study. As shown in **Fig. 2**, the DDC we consider uses an insulating full-bridge configuration. The primary side consists of the P and N power-supply lines, bypass capacitors, four transistors (vertical MOSFETS in TO-3P packages), and snubber capacitors connected between the drain and source of each transistor. To ensure that the internal diode within the transistors does not turn on during dead-time intervals, a capacitor designed to achieve zero-current switching (ZCS) is inserted between the transformer and the common terminal shared by the source of M_1 and the drain of M_2 (the midpoint of the upper-lower arm). The primary and secondary sides of the circuit are insulated from each other by a center-tapped transformer with a winding ratio of 7:1; the secondary side consists of rectifier diodes and a smoothing filter and achieves full-wave rectification. We chose the size of the circuit board on which the DDC is constructed to be 20 cm × 20 cm, approximately the size of a standard DDC for automotive applications.

Figure 3 shows the pathway for operating currents flowing through the primary side of Fig. 2. As shown in Figs. 3(a) and (b), of the four transistors on the primary side, M_1 is synchronized with M_4, while M_2 is synchronized with M_3; by alternately turning these on and off, a DC voltage is converted to an AC voltage. A dead-time interval, with all transistors in the off-state, is inserted between the states of Figs. 3(a) and (b) to ensure that the power-supply terminals are never shorted together. The secondary side of the circuit performs full-wave rectification and smoothing of the AC voltage appearing at the secondary side of the transformer, yielding the desired DC output voltage.

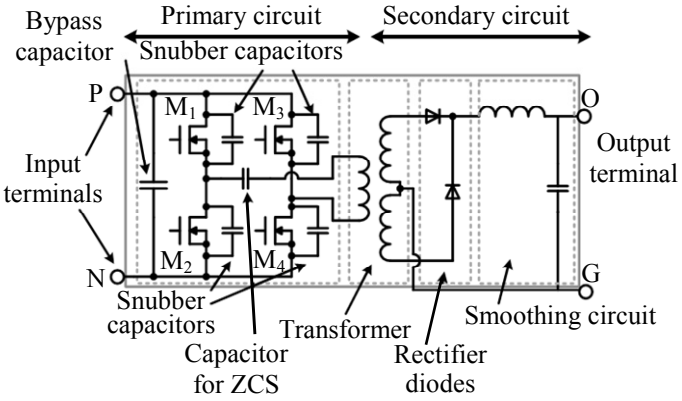


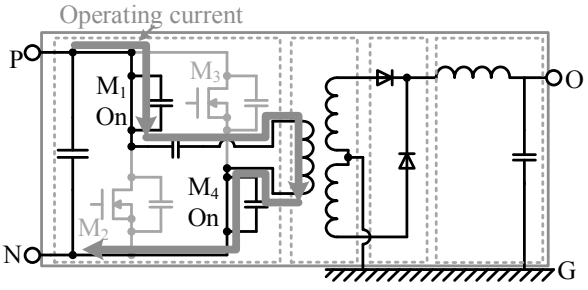
Fig. 2 Circuit diagram of the DC-DC converter.

3. An Analysis of Noise Sources and Mechanisms Responsible for Common-mode Input Voltages in the Idealized Circuit

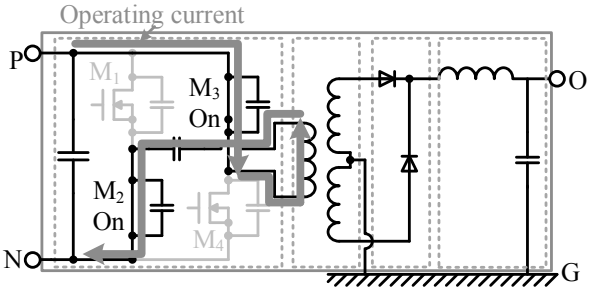
3. 1 Idealized Analysis of the Noise Source V_d

In this section, we analyze noise sources in the DDC of Fig. 2 in two ways: (a) by studying the timing of voltage fluctuations and common-mode voltages between the P and N power-supply lines when the circuit is in operation, and (b) by theoretically analyzing the mechanisms responsible for producing noise.

We begin with item (a). For a DDC installed in a vehicle, it is difficult to analyze noise in the DDC portion of the circuitry alone, and thus we constructed the evaluation circuit shown in **Fig. 4**. In Fig. 4 we have extracted just the portions of a vehicle installation that are relevant for the purposes of our study; beneath the housing of the DDC we place an aluminum slab that simulates the effect of the



(a) When M_1 and M_4 are turned on.



(b) When M_2 and M_3 are turned on.

Fig. 3 Operating current pathway in primary side of the DC-DC converter.

vehicle body, and we measure common-mode voltages with respect to this slab, which we term the aluminum ground. We have minimized the conversion of normal-mode currents to common-mode currents due to impedance mismatches between the power-supply lines and/or batteries. To ensure that the load impedance remains constant for frequencies as high as 150 MHz, we inserted a line impedance stabilization network (LISN; specifications listed in **Table 1**) between the DDC and the battery; in addition, we used wires of the same length for the P and N connections between DDC and LISN, we ensured that all wires lie the same distance from the aluminum ground, and that the impedance balancing did not vary between the DDC input terminals and the LISN. We were able to clamp the DDC-LISN interconnect wires to current probes (ETS-Lindgren 94111-1), and we kept the distance between the DDC input terminals and the point at which we observed V_{cin} (the LISN noise terminal/voltage measurement terminal) as short as possible—below 10 cm—to minimize measurement errors caused by phase shifts. We used copper tape to connect the LISN and DDC housing (made of aluminum) to the aluminum ground. To simulate the typical electrical load in a vehicle, we connected a 1.4 Ω electronic load (Kikusui Electronics Corp. PLZ1004W) between the aluminum ground and the output terminal of the secondary side and set the load current at 10 A. We inserted ferrite cores to reduce the noise current flowing between the electronic load and the commercial power supply.

Using the test circuit of Fig. 4, we made synchronized measurements of the waveforms of the common-mode voltage (V_{cin}) at the input terminal, the voltage fluctuation between the P and N power-supply lines (V_d), and the gate-source and drain-source voltages (V_{gs}, V_{ds}) of each transistor. V_{cin} was measured using an oscilloscope (Tektronix DPO7104C) connected to the LISN with a 50 Ω input impedance. The V_{gs} and V_{ds} waveforms of transistors M_1 and M_2 were measured using a high-voltage differential probe (Tektronix THDP0200). To measure V_d, we connected a high-voltage differential probe (Tektronix TDP1000) to the P and N lines through 10 nF capacitors to eliminate DC components. The trigger source for these waveform measurements was the V_{gs} waveform of M_2 (V_{gs2}). The other voltage waveforms were measured with the V_{gs2} waveform serving as a reference. The measurement results are shown in **Fig. 5**. The waveforms for transistors M_3 and M_4 are similar to those for M_2 and M_1 and are omitted from this plot. From Fig. 5, we see that V_d arises from the turn-on and turn-off of the various transistors in the circuit, and that V_{cin} arises in synchronization with V_d; also, the peak voltage of the V_{cin} waveform is larger for turn-on than for turn-off.

We next use the circuit in **Fig. 6** to analyze the mechanisms responsible for producing the noise source V_d. This circuit is obtained by extracting the bypass capacitor to the first arm of the full-bridge circuit shown in Fig. 4. In Fig. 6, C_{sm} and L_{Csm} are respectively the capacitance and parasitic inductance of the bypass capacitor, while L_{PP}, L_{PG}, R_{PP} and R_{PG} are the parasitic inductances and parasitic resistances of the wiring pattern from the bypass capacitor to the first upper/lower arm.

When M_1 turns on, M_2 is in the off state. In this state, the drain-source capacitance C_{off} of M_2 is the sum of the transistor output capacitance C_{oss} and the snubber capacitance C_{snu}:

$$C_{off} = C_{oss} + C_{snu}. \quad (3)$$

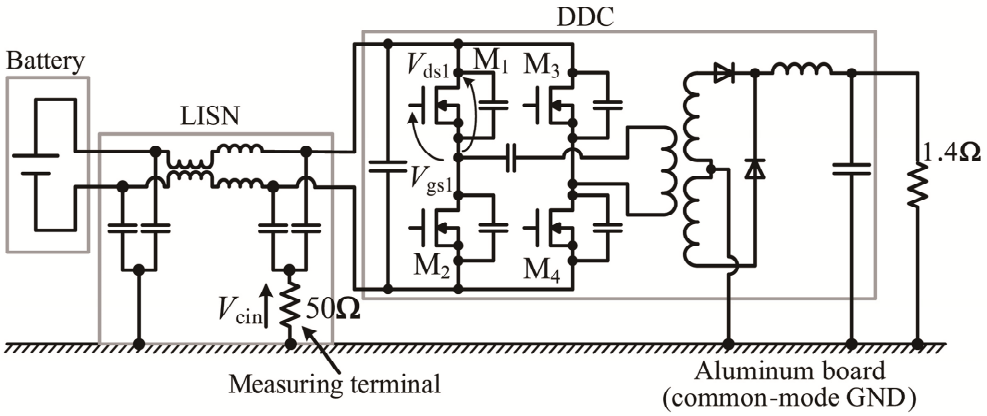


Fig. 4 Evaluation circuit for measurement of voltage waveforms.

When M_1 turns on, V_{ds1} changes from approximately 100 V to 0 V. We describe this temporal variation in V_{ds1} using a ramp function $v_{ds1}(t)$, defined by

$$v_{ds1}(t) = k_v t. \tag{4}$$

We simplify the circuit of Fig. 6 to yield the circuit of **Fig. 7**. Because the capacitances C_{sm} and C_{off} appear in series and $C_{sm} >> C_{off}$, we neglect C_{sm} in Fig. 7. The components of the circuit of Fig. 7 are related to those of Fig. 6 by

$$L = L_{PP} + L_{PG} + L_{Csm}, \tag{5}$$

$$R = R_{PP} + R_{PG}. \tag{6}$$

Table 1 Specs of the LISN.

Frequency range	1 M-150 MHz
Impedance of lines	50 Ω
Connection of lines	Delta connection
Measuring terminal	BNC-J connector

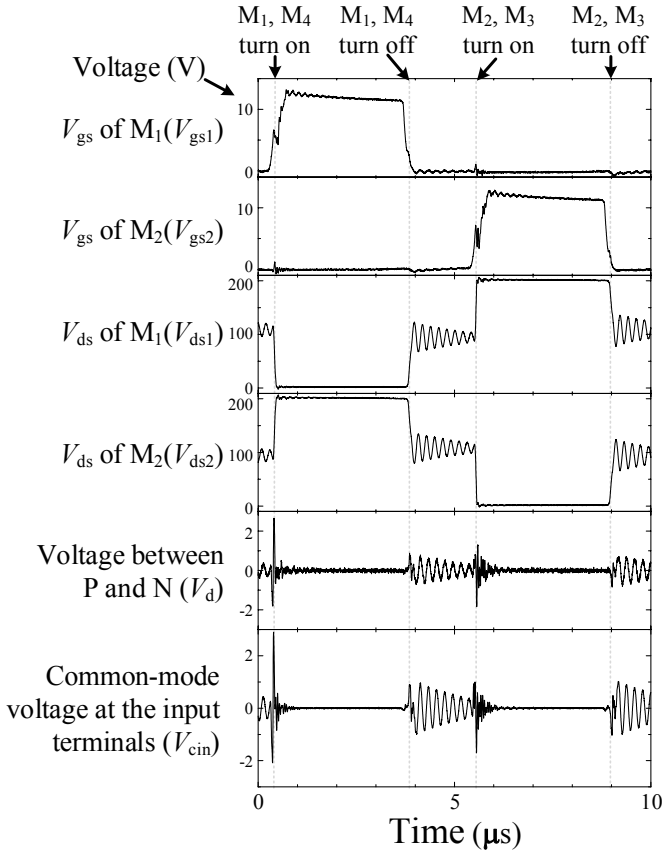


Fig. 5 Experimental results of each voltage wave form.

By Kirchhoff's voltage law, the sum of the voltages across each component reads

$$v_{ds1}(t) + v_{ds2}(t) + v_L(t) + v_R(t) = 0. \tag{7}$$

In Fig. 7, $v_d(t)$ is a source of noise voltage between the P and N lines, as we now derive. First, denoting the input and output voltages by $v_{ds1}(t)$ and $v_{ds2}(t)$ respectively, the transfer function $G(s)$ reads

$$G(s) = \frac{v_{ds2}(s)}{v_{ds1}(s)} = -\frac{\dfrac{1}{sC_{off}I(s)}}{sL + R + \dfrac{1}{sC_{off}}I(s)}. \tag{8}$$

Here, $V_{ds1}(s)$, $V_{ds2}(s)$, and $I(s)$ are the Laplace transforms of $v_{ds1}(t)$, $v_{ds2}(t)$, and $i(t)$. Putting

$$\alpha = \frac{R}{2L}, \tag{9}$$

$$\omega_0 = \frac{1}{\sqrt{LC_{off}}}. \tag{10}$$

In Eq. (8), the transfer function reads

$$G(s) = -\frac{\omega_0^2}{s^2 + 2\alpha s + \omega_0^2}. \tag{11}$$

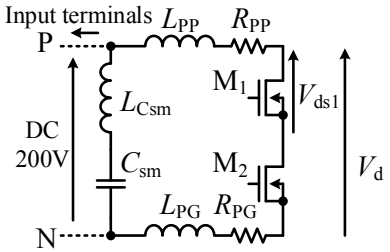


Fig. 6 Circuit from the bypass capacitor to the arm of full bridge circuit.

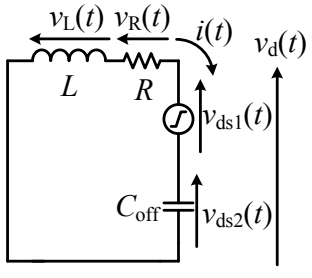


Fig. 7 Condensed circuit of Fig. 6.

Also, we may write

$$I(s) = sC_{\text{off}}V_{\text{ds2}}(s), \tag{12}$$

$$V_{\text{ds2}}(s) = G(s)V_{\text{ds1}}(s), \tag{13}$$

$$V_{\text{ds1}}(s) = \frac{k_{\text{v}}}{s^2}, \tag{14}$$

and, using Eqs. (11)-(14) to solve for $I(s)$, we have

$$I(s) = -k_{\text{v}}C_{\text{off}}\left(\frac{1}{s} - \frac{(s+\alpha)+\alpha}{(s+\alpha)^2+\beta^2}\right), \tag{15}$$

where

$$\beta = \sqrt{\omega_0^2 - \alpha^2} = \sqrt{\frac{1}{LC_{\text{off}}} - \frac{R^2}{4L^2}}\ . \tag{16}$$

For $t > 0$, the inverse Laplace transform of Eq. (15) yields $i(t)$:

$$i(t) = -k_{\text{v}}C_{\text{off}}\left\{1 - e^{-\alpha t}\left(\cos\beta t + \frac{\alpha}{\beta}\sin\beta t\right)\right\}. \tag{17}$$

Because we have $v_{\text{d}}(t) = v_{\text{ds1}}(t) + v_{\text{ds2}}(t)$, from Eq. (7) we find

$$v_{\text{d}}(t) = -\left(v_{\text{R}}(t) + v_{\text{L}}(t)\right). \tag{18}$$

In the DDC circuit board considered here, R is on the order of a few milliohms, while L is on the order of tens of nanohenries, and thus we have $\omega L >> R$ at FM-radio frequencies (here ω is the angular frequency). Thus, we have $v_{\text{L}}(t) >> v_{\text{R}}(t)$ and Eq. (18) may be simplified to read

$$v_{\text{d}}(t) = -v_{\text{L}}(t)\ . \tag{19}$$

Also, from (17), $v_{\text{d}}(t)$ takes the form

$$v_{\text{d}}(t) = -L\frac{di(t)}{dt} = -k_{\text{v}}LC_{\text{off}}\frac{\alpha^2+\beta^2}{\beta}e^{-\alpha\beta}\sin\beta t\ . \tag{20}$$

Using (9) and (16) to simplify (20) yields

$$v_{\text{d}}(t) = \frac{k_{\text{v}}}{\beta}e^{-\alpha t}\sin\beta t\ . \tag{21}$$

With C_{off} on the order of a few nanofarads and values of R, L as discussed above, from Eq. (16) the quantity β is given approximately by

$$\beta = \sqrt{\frac{1}{LC_{\text{off}}} - \frac{R^2}{4L^2}} \approx \frac{1}{\sqrt{LC_{\text{off}}}}\ . \tag{22}$$

Then Eq. (20) reads

$$v_{\text{d}}(t) = k_{\text{v}}LC_{\text{off}}e^{-\alpha t}\sin\beta t\ . \tag{23}$$

Equation (23) says that, if $v_{\text{ds1}}(t)$ (the transistor drain-source voltage) varies linearly in time during turn-on and turn-off, the voltage $v_{\text{d}}(t)$ between the P and N lines is a damped sinusoid whose amplitude is proportional to L, C_{off}, and the quantity k_{v}, which measures the rate of change of the voltage V_{ds}. This explains the mechanism responsible for the noise source V_{d} arising between the P and N lines due to transistor switching in the DDC.

Comparing the magnitudes of the V_{d} signals arising upon turn-on and upon turn-off in Fig. 5, we see that the former exceeds the latter. This is because the quantities C_{off} and dV_{ds}/dt (which correspond to k_{v} in Eq. (23)) are larger during turn-on than during turn-off. It is known that, for power MOSFETS in general, dV_{ds}/dt is larger during turn-on than during turn-off.[13] Also, C_{off} is larger during turn-on than during turn-off due to the voltage dependence of C_{oss}. We conclude that these factors explain the larger V_{d} magnitudes observed during turn-on than during turn-off in Fig. 5.

3. 2 Analysis of the Origin of the Common-mode Voltage at the Input Terminals (V_{cin})

In the previous section, we obtained analytical expressions describing the V_{d} response. In this section we investigate whether or not the common-mode voltage at the input terminals (V_{cin}) arises—as in Ref. 12—from V_{d} and an imbalance in the impedances of the power-supply lines. **Figure 8** shows a schematic diagram of the primary-side DDC circuitry, including parasitic elements. As shown in this figure, the parasitic elements include the parasitic inductances L_{p}, L_{n} of the primary-side power-supply

interconnect pattern as well as the parasitic capacitances C_p, C_n between the power-supply lines and aluminum ground. The locations within the printed circuit board at which L_p, L_n, C_p, and C_n are indicated schematically in **Fig. 9**.

In Fig. 8, if the impedance of the bypass capacitor C_x is sufficiently small, and the voltage gap between the P and N terminals is small enough to be negligible at FM-radio frequencies, then the circuit of Fig. 8 may be approximated by the bridge circuit of **Fig. 10**. In Fig. 10, Z_R is the common-mode impedance from the bypass capacitor to the aluminum ground and I_{cin} is the common-mode current flowing into the input terminals. V_{cin} is the common-mode voltage at the input terminal referenced to the aluminum ground, defined as the voltage gap V_1 - V_2 between points 1 and 2. If I_1 and I_2 are sufficiently large compared to I_{cin}, then V_{cin} may be expressed in the form

$$V_1 - V_2 = V_{cin} = \frac{L_p C_p - L_n C_n}{(L_p + L_n)(C_p + C_n)} V_d \quad (24)$$

From Eq. (24) we see that, assuming frequency-independent inductances and capacitances, V_{cin} does not depend on frequency; it is determined by V_d and the parasitic inductances of P and N power-supply lines and capacitances of the supply lines (L_p, L_n, C_p, C_n). In this paper we will refer to the coefficient of V_d in Eq. (24), which measures the imbalance in the impedance of the power-supply lines, as the balance factor (BF), defined by

$$BF = \frac{L_p C_p - L_n C_n}{(L_p + L_n)(C_p + C_n)} . \quad (25)$$

If BF vanishes—that is, if the condition

$$L_p C_p - L_n C_n = 0 \quad (26)$$

is satisfied—then we say that the impedances of the power-supply lines are *balanced*; in this case we have $V_{cin} = 0$.[12]

As this discussion shows, the impedance balance is determined by the matching of impedances among the various components comprising the circuitry between the noise sources and C_x, and does not depend on the size of the DDC circuit board. In an actual DDC, these components will lie within a spatial region whose extent is determined by the lumped constant for the FM-radio band (at 108 MHz, 1/20 wavelength corresponds to 14 cm). Thus the results of the analysis presented above are generally applicable.

Next, we experimentally analyze the impact of BF on V_{cin}. **Figure 11** shows a schematic of the test circuit we use, while **Fig. 12** shows the circuit board fabricated for our experiments. In this circuit we have retained only the structural components necessary to give rise to the noise source (V_d) for the common-mode input voltage V_{cin}. The circuit contains a single upper/lower arm structure

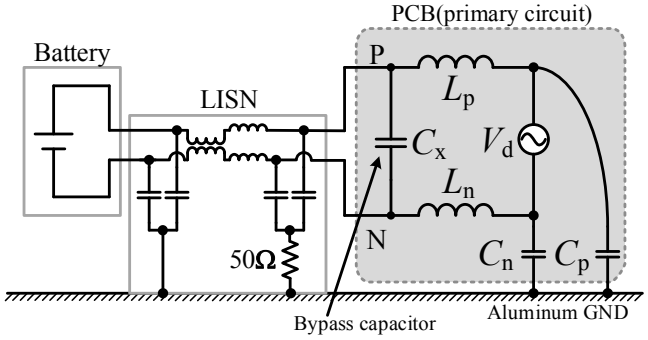


Fig. 8 Primary circuit of the DC-DC converter including parasitic impedances.

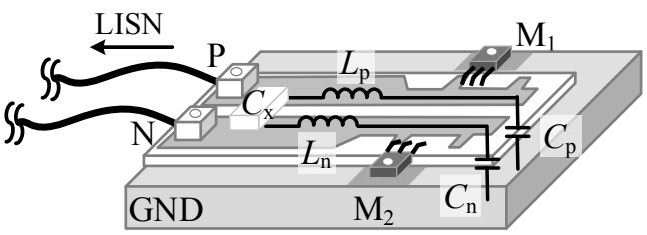


Fig. 9 Schematic view of the parasitic impedances on the PCB of the DC-DC converter.

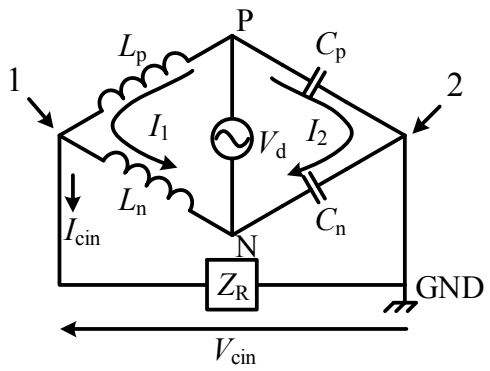


Fig. 10 Equivalent circuit for the primary circuit of the DC-DC converter.

comprised of two transistors (M_1, M_2); these are switched as in the actual DDC to produce V_d. To suppress the common-mode current flowing in the transistor control circuit, we have inserted a common mode absorbing device (CMAD; TESEQ CMAD-10) between the circuit board and the control circuit. To isolate the effect of *BF* in our analysis, we omit the transformer and the output-side circuitry.

For this experiment we used a four-layer circuit board. To ensure that the bypass capacitors have low impedance at FM-radio frequencies, we connected six ceramic capacitors in parallel to yield a total capacitance of 20 nF. The P and N power-supply lines lie on the same layer and are laid out symmetrically to ensure that the parasitic inductances and capacitances in these lines satisfy the conditions of Eq. (26). We used this circuit board to investigate the dependence of V_{cin} on *BF*. For this purpose, we attached at positions on the circuit board corresponding to L_p, L_n, C_p, and C_n shown in Fig. 12, chip components whose parasitics are ten times or larger than those of the circuit board itself. By adjusting the values of these components, we varied the value of *BF*. In one particular case, we fixed the values $L_p = L_n = 150$ nH, $C_p = 110$ pF, varied C_n over a set of 5 values (67, 100, 110, 120, and 147 pF), and measured V_{cin} for each case. With these component values, the quantity *BF* ranges from −0.07 to 0.12, with $BF = 0$ corresponding to the balanced condition. We used an impedance analyzer (Agilent Technologies 4294A) to measure the capacitances and inductances of the chip components and confirmed that these were constant within the FM-radio band, whereupon we treat them here as frequency-independent constant values.

Figure 13 compares the frequency dependence of V_{cin}, as observed with the system in the balanced configuration ($BF = 0$), to that observed for a case in which the balance was offset ($BF = 0.12$). We characterized the frequency dependence of V_{cin} by using a spectrum analyzer (Tektronix RSA3408B) to measure the LISN noise terminal voltage. Experimental conditions are listed in **Table 2**. From **Fig. 13**, we see that V_{cin} is some 20 dB smaller in the balanced configuration than in the imbalanced configuration. **Figure 14** shows the *BF* dependence of V_{cin} at two characteristic FM-radio frequencies of 80 MHz and 100 MHz. In this figure, circles denote experimental results, while the solid line indicates the theoretical prediction of Eq. (24). Here, we used Eq. (24) to determine the value of V_d that yields agreement with the measurement results for $BF = 0.12$. We then used this value of V_d to compute values of V_{cin} under other conditions. Our

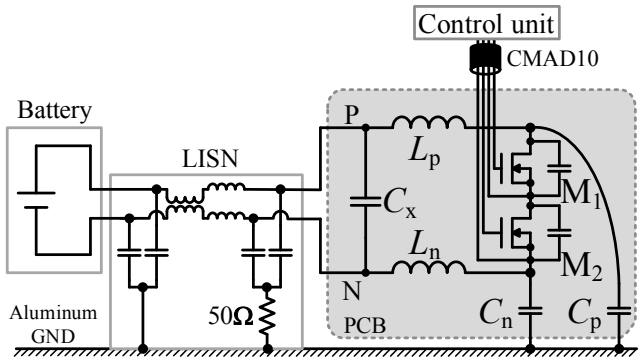


Fig. 11 Experimental circuit to evaluate impedance balance.

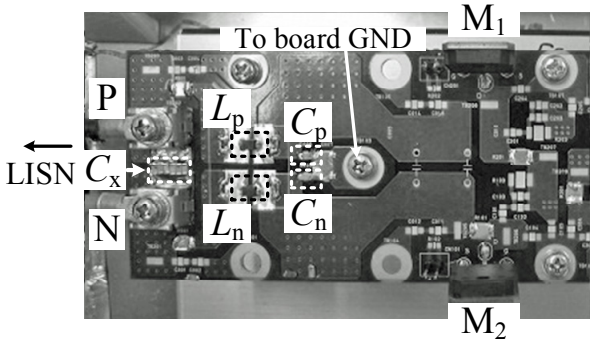


Fig. 12 Picture of the PCB in Fig. 11.

Table 2 Setting of spectrum analyzer.

Frequency range	20 M-150 MHz
Number of points	16001
Resolution band width	100 kHz
Video band width	Auto setting

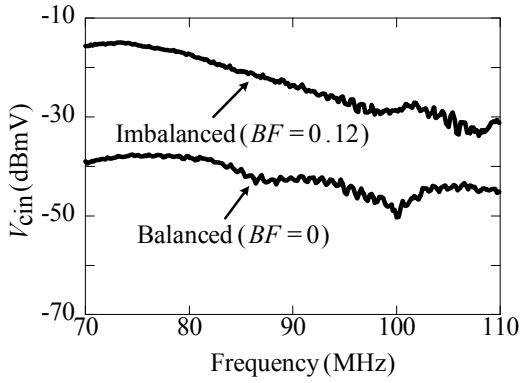
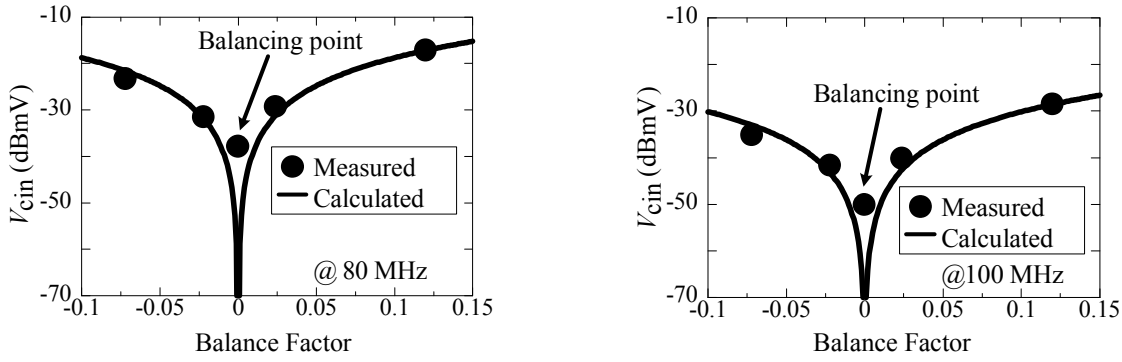


Fig. 13 Comparison of frequency response of V_{cin} between balance condition and imbalance one.



(a) Results at 80 MHz (b) Results at 100 MHz

Fig. 14 V_{cin} dependence on *BF*.

results indicate qualitative agreement of theoretical predictions and experimental measurements, demonstrating that, at FM-radio frequencies, the common-mode voltage at the input terminals of the DDC studied here is approximately expressed by Eq. (24).

4. Analyzing the Effect on V_{cin} of the Parasitic Capacitance between Ground and the Arm Midpoint (C_s)

As is evident in Fig. 14, the experimentally measured value of V_{cin} in the balanced configuration is larger than the theoretically predicted value. This indicates the presence of factors other than the power-supply-line impedances of Eq. (24) that contribute to determining V_{cin}. These factors, not expressed by Eq. (24), include (i) parasitic inductances in C_p and C_n, (ii) parasitic capacitance in L_p and L_n, and (iii) parasitic capacitance between aluminum ground and the midpoint of the upper/lower arm. The impedance measurements discussed above demonstrate that the effects of factors (i) and (ii) are small at FM-radio frequencies. Therefore, in this section, we investigate the effect of factor (iii), parasitic capacitance between the aluminum ground and the midpoint of the upper/lower arm.

In the bridge circuit of Fig. 10, V_d was the only source of noise due to transistor switching between the P and N power-supply lines. In reality, however, as shown in **Fig. 15**, the midpoint of the upper/lower arm is also connected to the transformer and the control circuitry, forming a parasitic capacitance between this point and aluminum ground. A parasitic capacitance is also

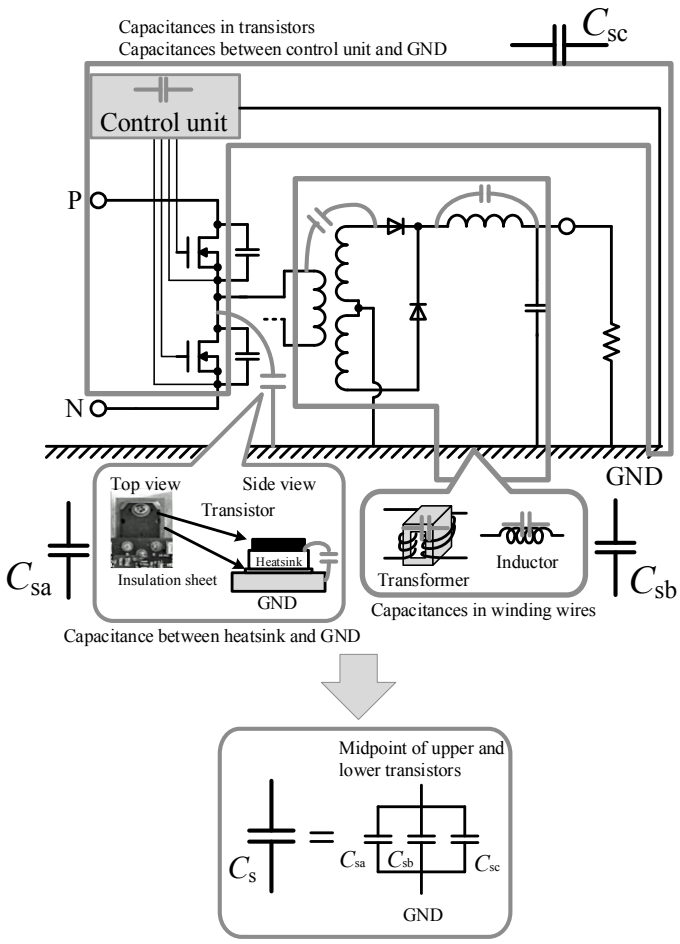


Fig. 15 Components of C_s.

present between the transistor drain terminals and the heat sink, and the heat sink is connected to the aluminum ground with a low impedance. Here we use the symbol C_s to refer collectively to the total parasitic capacitance, arising from all sources, between the upper/lower arm midpoint and aluminum ground.

With a parasitic capacitance C_s present at the upper/lower arm midpoint, the alternating on/off switching of M_1 and M_2 modifies the bridge circuit as shown in **Fig. 16**. As this figure illustrates, C_s appears in parallel with C_p when M_1 is on and with C_n when M_2 is on. Thus, Eq. (25) is modified to read

$$BF = \frac{L_p(C_p + C_s) - L_n C_n}{(L_p + L_n)(C_p + C_n + C_s)}, \quad (27)$$

when M_1 is on, and to read

$$BF = \frac{L_p C_p - L_n(C_n + C_s)}{(L_p + L_n)(C_p + C_n + C_s)}, \quad (28)$$

when M_2 is on. During the transient state accompanying turn-on and turn-off, *BF* attains values that are intermediate between those given by Eqs. (27) and (28). From these equations we see that, even if the impedance of the power-supply lines is balanced, this balance is nonetheless destroyed to the extent that C_s is present, leading to an increase in V_{cin}. We propose that this explains the experimental observation, evident in Fig. 14, that measured values of V_{cin} in the balanced configuration (*BF* = 0) are larger than theoretical predictions. Of course, values of C_s differ from one power converter to another, but C_s must always be present on physical grounds and will be a factor tending to offset the impedance balance, even in power converters other than the test system we consider here.

The test circuit in Fig. 11 was used to check this experimentally. We first estimated C_s for the circuit of Fig. 11. To simplify the estimation of C_s, we positioned the transistors at 90-degree angles so that their drain side did not contact the heat sink, allowing us to neglect the parasitic capacitance between drain and heat sink. Also, the insertion of the CMAD allows us to neglect the parasitic capacitance between the control circuitry and the aluminum ground. Thus, in this circuit, C_s consists of only the parasitic capacitance to aluminum ground plus that of the wiring pattern of the source of M_1 and the drain of M_2; using Ansys Q3D Extractor, we estimated its value at approximately 10 pF.

In our experiments, we used the values L_p = L_n = 150 nH and considered three values (470 pF, 200 pF, 110 pF) for C_p and C_n. By choosing the same values for C_p and C_n, we balanced impedances to allow the relative influence of C_s to be varied. With these parameters, the values of *BF* in Eqs. (27) and (28) ranged from 0.005 to 0.021. **Figure 17** shows the measurement results for V_{cin} in this case. Because it is difficult to realize the condition *BF* = 0 experimentally, our results here are for the smallest measurable value of *BF* (*BF* = 0.005). From Fig. 17 we confirm that, as the effect of C_s increases, *BF* increases and V_{cin} worsens. Figure 18 compares, at a frequency of 80 MHz, the *BF* dependence of V_{cin} with C_s taken into account against the predictions of Eqs. (27) and (28). For these calculations, we determine the value of V_d that yields agreement with measured results for *BF* = 0.021, then use this value of V_d to compute V_{cin} under other conditions. In **Fig. 18**, circles and triangles respectively indicate measured values and theoretical predictions. The measurements approximately agree with the theoretical calculations, confirming the soundness of

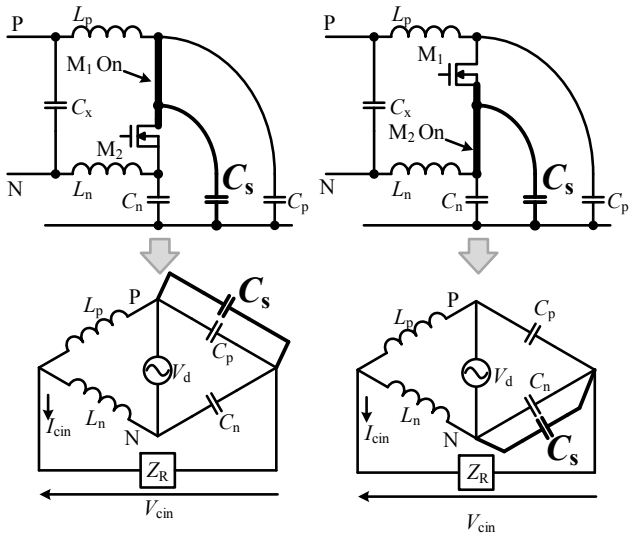


Fig. 16 C_s connection corresponding to the switching conditions.

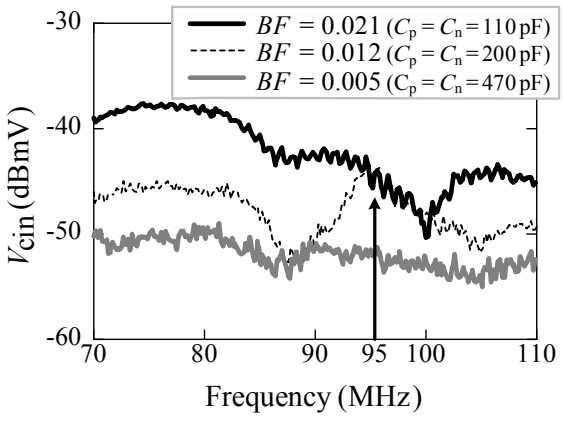


Fig. 17 Comparison of frequency response of V_{cin} when C_p and C_n are changed.

our analytical results.

On the other hand, considering the results of Fig. 17 over the full FM-radio band (76-108 MHz) analyzed in this study, we see that, for $BF = 0.12$, we fail to achieve sufficient suppression of V_{cin} in the frequency range 90-100 MHz, in contrast to what is found at 80 MHz. We attribute this to the effect of a resonance arising at 95 MHz, indicated by the arrow in Fig. 17. Assuming a series resonance of C_p/C_n with a parasitic inductance, using the capacitance value (200 pF) and the 95 MHz resonance frequency we compute an inductance of approximately 15 nH. We attribute this to the inductance arising from interconnect wiring pattern of the DDC circuit board plus the parasitic inductance of the chip components. In future work we plan to carry out a detailed analysis of this resonance by studying the variation of the resonance frequency as the values of the aforementioned capacitances and inductances are varied.

From these findings we see that, even if the impedance of the power-supply lines is balanced, the balance may nonetheless be offset if C_s grows large relative to C_p and C_n. In addition, in order to minimize the effect of V_{cin}, the values of capacitances C_p and C_n must be chosen sufficiently large compared to C_s.

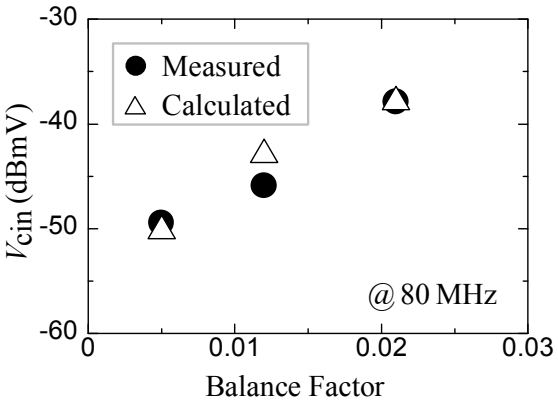


Fig. 18 V_{cin} dependence on BF.

5. Conclusions

In this study we considered a full-bridge insulated DDC and analyzed the mechanisms responsible for producing a common-mode voltage V_{cin} at the input terminals. Our findings were as follows:

- The temporal variation of the drain-source voltages of the transistors in the primary-side circuitry during turn-on and turn-off produces a voltage between the P and N power-supply lines that takes the form of a damped sine wave and constitutes a source of noise.
- V_{cin} is determined by the product of V_d and the impedance balance factor (BF) of the power-supply lines.
- Even if the impedance of the power-supply lines is balanced, the balance is offset by the parasitic capacitance C_s from the midpoint of the upper/lower arm to ground, causing V_{cin} to increase.
- To minimize BF and effectively reduce V_{cin}, the capacitances C_p and C_n must be large relative to C_s.

In future work we plan to apply the analytical results of this study to an actual DDC to test the effects discussed in this paper.

References

(1) Paul, C. R., "A Comparison of the Contributions of Common-mode and Differential-mode Currents in Radiated Emissions", *IEEE Trans. Electromagn. Compat.*, Vol. 30, No. 2 (1989), pp. 189-193.

(2) Paul, C. R., *Introduction to Electromagnetic Compatibility* (2006), pp. 509-518, Wiley-Interscience.

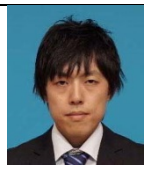
(3) Ogasawara, S., Fujita, H. and Akagi, Y., "Modeling and Analysis of High-frequency Leakage Currents Caused by Voltage-source PWM Inverters", *IEEJ Trans. Ind. Appl.* (in Japanese), Vol. 115, No. 1 (1995), pp. 77-83.

(4) ISO 6469-3: 2011. Electrically Propelled Road Vehicles – Safety Specifications – Part 3: Protection of Persons against Electric Shock.

(5) Kondo, Y., Izumichi, M., Yamamoto, T. and Hirano, N., "VHF Conducted Emission Simulation of Power Electronic Devices", *IEEJ Trans. Ind. Appl.* (in Japanese), Vol. 133, No. 5 (2013), pp. 510-517.

(6) Saito, M., Matsui, N., Masuzawa, T., Taki H. and Fujitsuna, M., "A EMI Noise Suppression Method for Power Electronics Circuits over VHF Region", *Pap. Tech. Meet. Intell. Transp. Systems* (in Japanese) (2009), No. 89, pp. 1-6.

(7) Hasegawa, H., Harada, K., Ishihara, Y. and Todaka, T., "An Examination of Radiation Noise Characteristics in DC-DC Converters", *Trans. Inst. Electron., Inf. Commun. Eng.* (in Japanese), Vol. J84-B (2001), No. 4, pp. 801-808.
(8) Shoyama, M., Li, G. and Ninomiya, T., "Balanced Switching Converter to Reduce Common-mode Conducted Noise", *IEEE Trans. Ind. Electron.*, Vol. 50, No. 6 (2003), pp. 1095-1099.
(9) Li, G., Ninomiya, T. and Syoyama, M., "Noise Reduction of Common-source Type Active-clamped DC-DC Converters", *IEEJ Trans. Ind. Appl.* (in Japanese), Vol. 123, No. 9 (2003), pp. 1037-1042.
(10) Kong, P., Wang, S., Lee, F. C. and Wang, Z., "Reducing Common-mode Noise in Two-switch Forward Converter", *IEEE Trans. Power Electron.*, Vol. 26, No. 5 (2011), pp. 1522-1533.
(11) Karvonen, A., Thiringer, T. and Futane, P., "Reduction of EMI in Switched Mode Converters by Shaped Pulse Transitions", *SAE Tech. Pap. Ser.*, No. 2007-01-0361.
(12) Mabuchi, Y., Nakamura, A., Hayashi, T., Ichikawa, K., Uno, T. and Mizuno, H., "A Feasibility Study for Reducing Common-mode Current on the Wire Harness Connected to Electronic Control Units", *Trans. Inst. Electron. Inf. Commnun. Eng. C* (in Japanese), Vol. J89-C, No. 11 (2006), pp. 854-865.
(13) Inaba, T., *Pawa MOSFET Katsuyo no Kiso to Jissai* (in Japanese) (2004), pp. 31-32, CQ *Shuppan*.



Atsuhiro Takahashi
Research Fields:
- Electro-magnetic Compatibility (EMC) for Hybrid Vehicle
- Analysis of Electromagnetic Field Using FEM
- Topology Optimization

Academic Societiy:
- The Institute of Electronics, Information and Communication Engineers

Hiroshi Tsukada
Research Field:
- Power Electronics

Academic Societies:
- The Institute of Electronics, Information and Communication Engineers
- IEEE

Takashi Kojima
Research Fields:
- Electromagnetic Interference in Hybrid Vehicles
- Power Electronics Simulation
- Power Device Modeling

Academic Degree: Dr.Eng.
Academic Society:
- The Institute of Electrical Engineers of Japan

Yoshiyuki Hattori
Research Fields:
- Electronic Devices for Automotive Application
- Electromagnetic Compatibility for Hybrid Vehicle

Academic Degree: Dr.Eng.
Academic Societies:
- Institute of Electronics, Information and Communication Engineers
- The Institute of Electrical Engineers of Japan
- Society of Automotive Engineers of Japan

Tsuyoshi Funaki*
Research Field:
- Power Electronics

Academic Degree: Ph.D.
Academic Societies:
- IEEE
- The Institute of Electronics, Information and Communication Engineers
- The Institute of Electrical Engineers of Japan

Osami Wada**
Research Fields:
- Electromagnetic Compatibility (EMC) of Electronic Circuits and Systems
- EMC Macro-models of Integrated Circuits

Academic Degree: Dr.Eng.
Academic Societies:
- IEEE
- The Institute of Electronics, Information and Communication Engineers
- The Institute of Electrical Engineers of Japan
- The Japan Institute of Electronics Packaging

Awards:
- 1906 Award, International Electrotechnical Commission, 2009.
- IEICE Fellow, 2012.
- Best Paper Award, IEICE Transactions on Communications, 2010

*Osaka University
**Kyoto University

